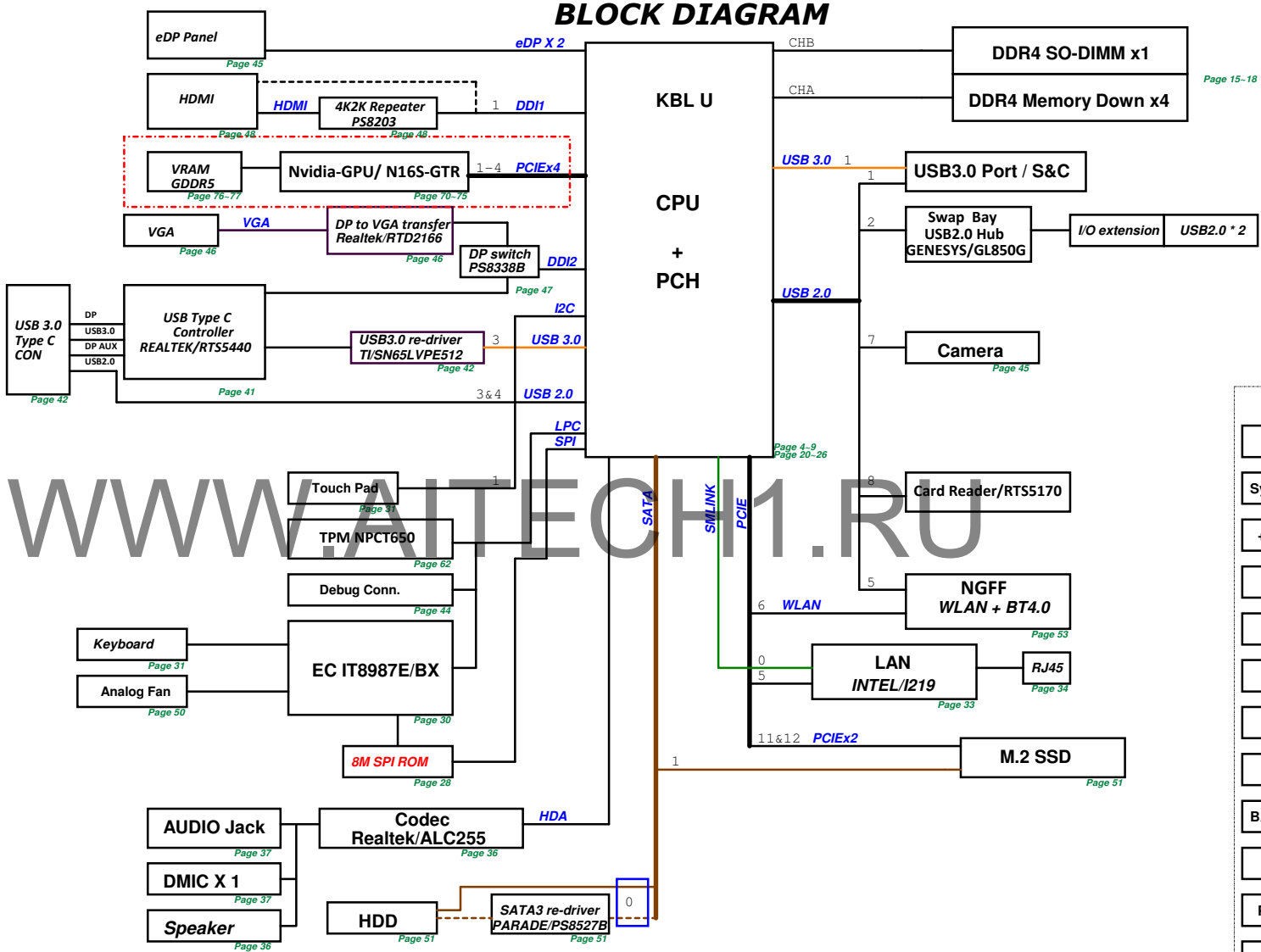
# P2 Kaby Lake U (2+2) Rev1.0

## SYSTEM PAGE REF.



## BLOCK DIAGRAM




### Power



### D.B.





<Variant Name>

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Title : Block Diagram
Engineer: Bill Yang

| Size | Project Name | Rev |
|---|---|---|
| BG1/HW3 | AQ5EB | 1.0 |
| Custom | | |

Date: Wednesday, August 23, 2017 Sheet 1 of 108

**Function Remove List:**

**1. Remove WIGIG**

**2. Remove NFC**

**3. Remove Touch Panel**

**4. Remove Finger Print**

**5. Remove G-Sencor**

**6. IO Board remove Smart Card Reader and one Port USB2**



<Variant Name>

PEGATRON Title :



Engineer:

Size A3 Project Name Rev1.1

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SKYLAKE-U symbol ReV0.53 #545316 / Ballout_Rev0_71 #543787 / PEGA local PN is 4201-0062000

+VCCIO +VCCIO 7,57,91
+VCCST_CPU +VCCST_CPU 5,7,9,25
+VCCSTG +VCCSTG 5,7
+3VS +3VS 4,17,20,21,22,23,24,28,30,31,32,36,37,41,42,45,46,47,48,50,51,53,57,61,62,67,91,92

DDI Port 1: HDMI

DDI Port 2: DP Switch

U0301A

HDMI_TXN2 48 E55 DDI1_TXN[0]
HDMI_TXP2 48 F55 DDI1_TXP[0]
HDMI_TXN1 48 E58 DDI1_TXN[1]
HDMI_TXP1 48 F58 DDI1_TXP[1]
HDMI_TXN0 48 F53 DDI1_TXN[2]
HDMI_TXP0 48 G53 DDI1_TXP[2]
HDMI_CLKN 48 F56 DDI1_TXN[3]
HDMI_CLKP 48 G56 DDI1_TXP[3]

DP2_TXN0 47 C50 DDI2_TXN[0]
DP2_TXP0 47 D50 DDI2_TXP[0]
DP2_TXN1 47 C52 DDI2_TXN[1]
DP2_TXP1 47 D52 DDI2_TXP[1]
DP2_TXN2 47 A50 DDI2_TXN[2]
DP2_TXP2 47 B50 DDI2_TXP[2]
DP2_TXN3 47 D51 DDI2_TXN[3]
DP2_TXP3 47 C51 DDI2_TXP[3]

DDI

HDMI_SCL_PCH 48 L13 GPP_E18/DDPB_CTRLCLK
HDMI_SDA_PCH 48 L12 GPP_E19/DDPB_CTRLDATA
DDPC_CTRLDATA N7 GPP_E20/DDPC_CTRLCLK
N8 GPP_E21/DDPC_CTRLDATA
N11 GPP_E22
N12 GPP_E23

DISPLAY SIDEBANDS

+VCCIO R0301 2 1% 1 24.9Ohm DP_COMP E52 eDP_RCOMP

940432
01V010000015

EDP

EDP_TXN[0] C47 EDP_TXN0 45
EDP_TXP[0] C46 EDP_TXP0 45
EDP_TXN[1] D46 EDP_TXN1 45
EDP_TXP[1] C45 EDP_TXP1 45
EDP_TXN[2] A45
EDP_TXP[2] B45
EDP_TXN[3] A47
EDP_TXP[3] B47

eDP x 2

EDP_AUXN E45 EDP_AUXN 45
EDP_AUXP F45 EDP_AUXP 45

EDP_DISP_UTIL B52

DDI1_AUXN G50
DDI1_AUXP F50
DDI2_AUXN E48 DP2_AUXN 47
DDI2_AUXP F48 DP2_AUXP 47
RSVD_1 G46
RSVD_2 F46

GPP_E13/DDPB_HPD0 L9 DPB_HPD 48
GPP_E14/DDPC_HPD1 L7 DP2_HPD 47
GPP_E15/DDPD_HPD2 L6 EXT_SMI#_R R0302 1 2 0Ohm EXT_SMI# EXT_SMI# 30,44
GPP_E16/DDPE_HPD3 N9 EXT_SCI#_R R0303 1 2 0Ohm EXT_SCI# EXT_SCI# 30
GPP_E17/EDP_HPD L10 eDP_HPD eDP_HPD 45

Pull down at connector side

eDP_BKLTEN R12 LCD_BKLTEN_PCH 21,45
eDP_BKLTCTL R11 LCD_BL_PWM_PCH 45
eDP_VDDEN U13 EDP_VDD_EN 45

+VCCST_CPU +VCCSTG +VCCST_CPU

R0311 1KOhm R0312 1KOhm R0313 49.9Ohm 1% @

U0301D

H_PROCHOT# R0314 1 1% 2 499Ohm 30 H_PECI_EC R0315 1 2 43Ohm TP_CATERR#_R D63 CATERR#
H_PECI A54 PECI
H_PROCHOT#_R C65 PROCHOT#
SP0301 H_THRMTRIP#_R C63 THERMTRIP#
T0310 SKTOCC# A65 SKTOCC#

CPU MISC

BPM#[0] C55
BPM#[1] D55
BPM#[2] B54
BPM#[3] C56

T0312 CPU_GP0 A6 GPP_E3/CPU_GP0
T0311 CPU_GP1 A7 GPP_E7/CPU_GP1
T0313 CPU_GP2 BA5 GPP_B3/CPU_GP2
T0314 CPU_GP3 AY5 GPP_B4/CPU_GP3

R0316 1% 2 49.9Ohm CPU_POPIRCOMP AT16 PROC_POPIRCOMP
R0317 1% 2 49.9Ohm PCH_POPIRCOMP AU16 PCH_OPIRCOMP
R0318 1% 2 49.9Ohm EDRAM_OPIO_RCOMP H66 OPCE_RCOMP
R0319 1% 2 49.9Ohm EOPIO_RCOMP H65 OPC_RCOMP

JTAG

PROC_TCK B61 XDP_TCLK 1 T0315
PROC_TDI D60 XDP_TDI_CPU 1 T0316
PROC_TDO A61 XDP_TDO_CPU 1 T0317
PROC_TMS C60 XDP_TMS_CPU 1 T0318
PROC_TRST# B59 XDP_TRST_CPU_N 1 T0319

PCH_JTAG_TCK B56 PCH_JTAG_TCLK 1 T0320
PCH_JTAG_TDI D59 PCH_JTAG_TDI 1 T0321
PCH_JTAG_TDO A56 PCH_JTAG_TDO 1 T0322
PCH_JTAG_TMS C59 PCH_JTAG_TMS 1 T0323
PCH_TRST# C61 PCH_TRST_CPU_N 1 T0324
JTAGX A59 XDP_TCLK_JTAGX 1 T0325

940432
01V010000015



30 THRO_CPU
Q0301 2N7002 R0341 2 1 0Ohm H_PROCHOT#
88 PROCHOT#
SP0325 2 1 0Ohm
80 VR_HOT#
R0320 2 1 0Ohm

R0341由EC control 觸發時的對地電阻也是要介於 70-200 ohm
(depends on under-shoot measurement result),預留0ohm是調整空間

DDPB_CTRLDATA has pull high at connector side

+3VS
HDMI_SDA_PCH R0304 1 @ 2 2.2KOhm
DDPC_CTRLDATA R0321 1 2 2.2KOhm

DDPB_CTRLDATA
DDPC_CTRLDATA
DDPD_CTRLDATA
- Internal weak pull down 20k ohm
- 0 : port is not detected
1 : port is deteccted

+3VS
EXT_SCI# R0307 1 2 10KOhm
EXT_SMI# R0308 1 2 10KOhm

Table 5-10. DDI Disabling and Termination Guidelines

| Port | Strap | How to Enable Port? | How to Disable Port? |
|---|---|---|---|
| Port 1 | DDPB_CTRLDATA | Pull up to 3.3 V with 2.2-k W ±5% resistor | No Connect |
| Port 2 | DDPC_CTRLDATA | Pull up to 3.3 V with 2.2-k W ±5% resistor | No Connect |

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BG1/HW3
Engineer: Bill Yang
Size Custom | Project Name AQ5EB | Rev 1.0
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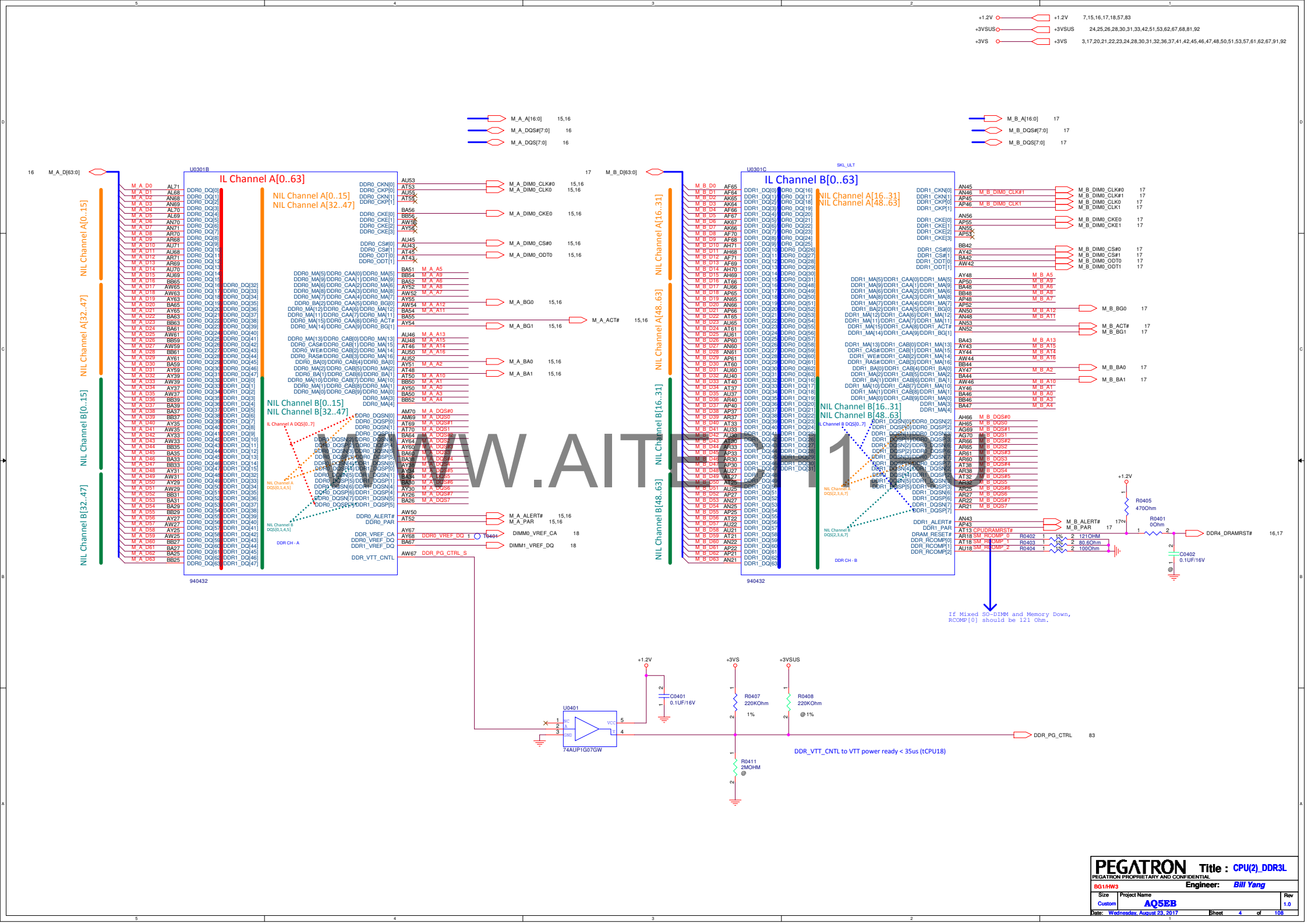




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Title : CPU(2)_DDR3L

BG1/HW3

Engineer: Bill Yang

| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 1.0 |

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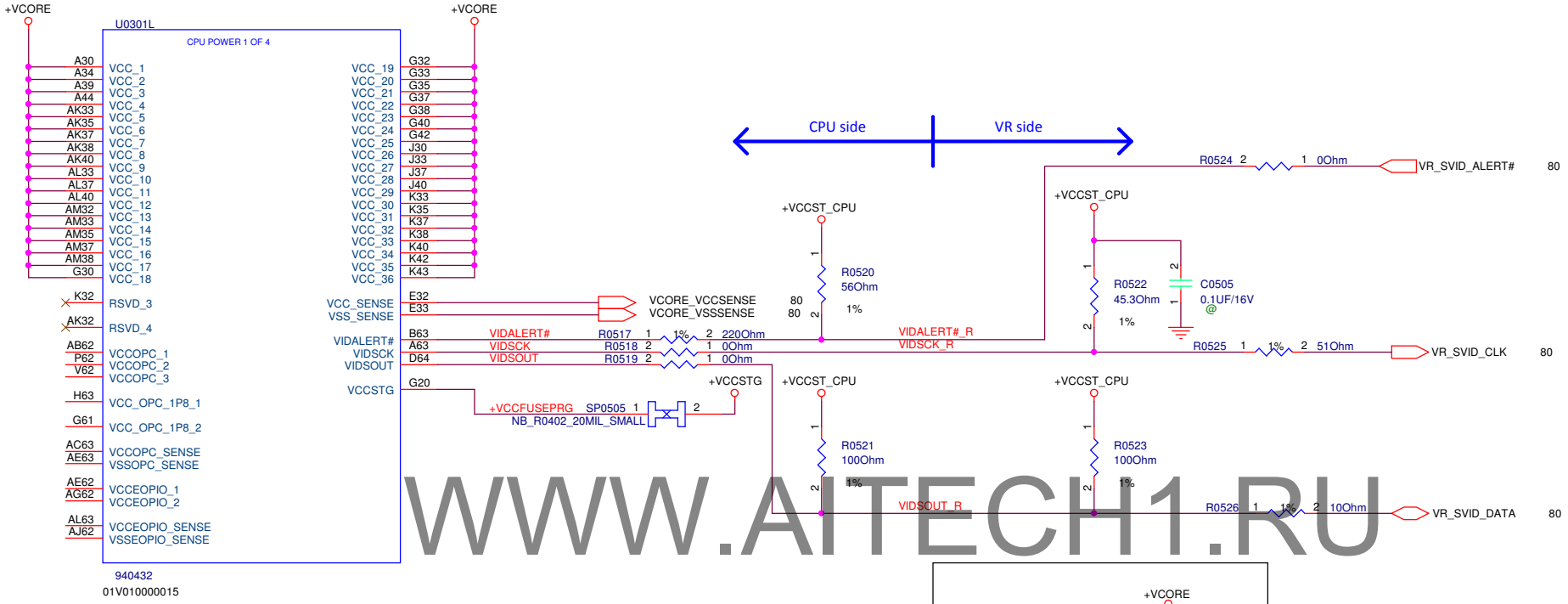
+VCORE +VCORE 57,80
+VCCSTG +VCCSTG 3,7
+VCCST_CPU +VCCST_CPU 3,7,9,25



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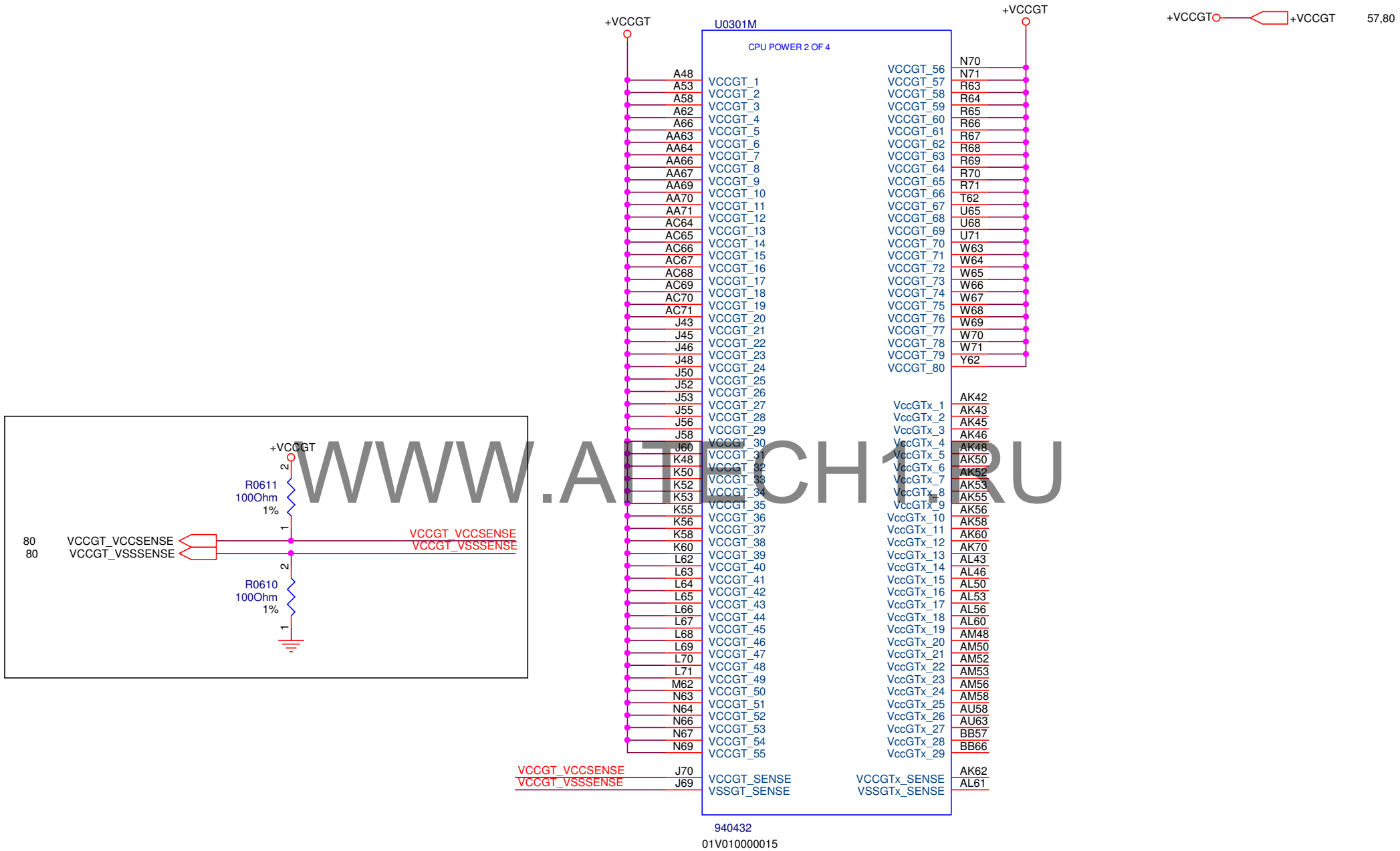
Title : CPU(3)_+VCCCORE
BG1/HW3
Engineer: Bill Yang
Size: Custom
Project Name: AQ5EB
Rev: 1.0
Date: Wednesday, August 23, 2017
Sheet 5 of 108



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Title : CPU(4)_+VCCGT

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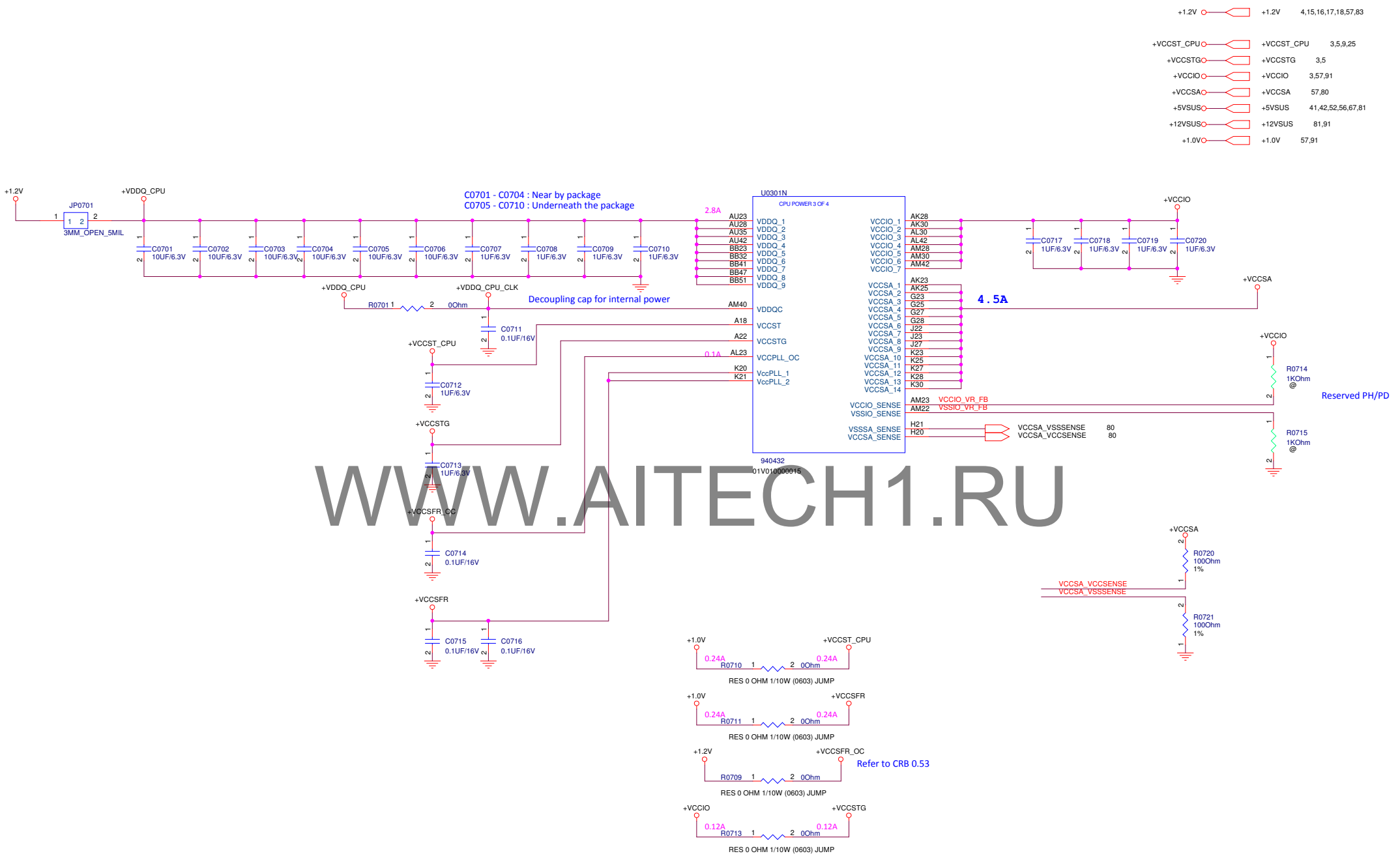
BG1/HW3

Engineer: Bill Yang

| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 1.0 |

Date: Wednesday, August 23, 2017 Sheet 6 of 108



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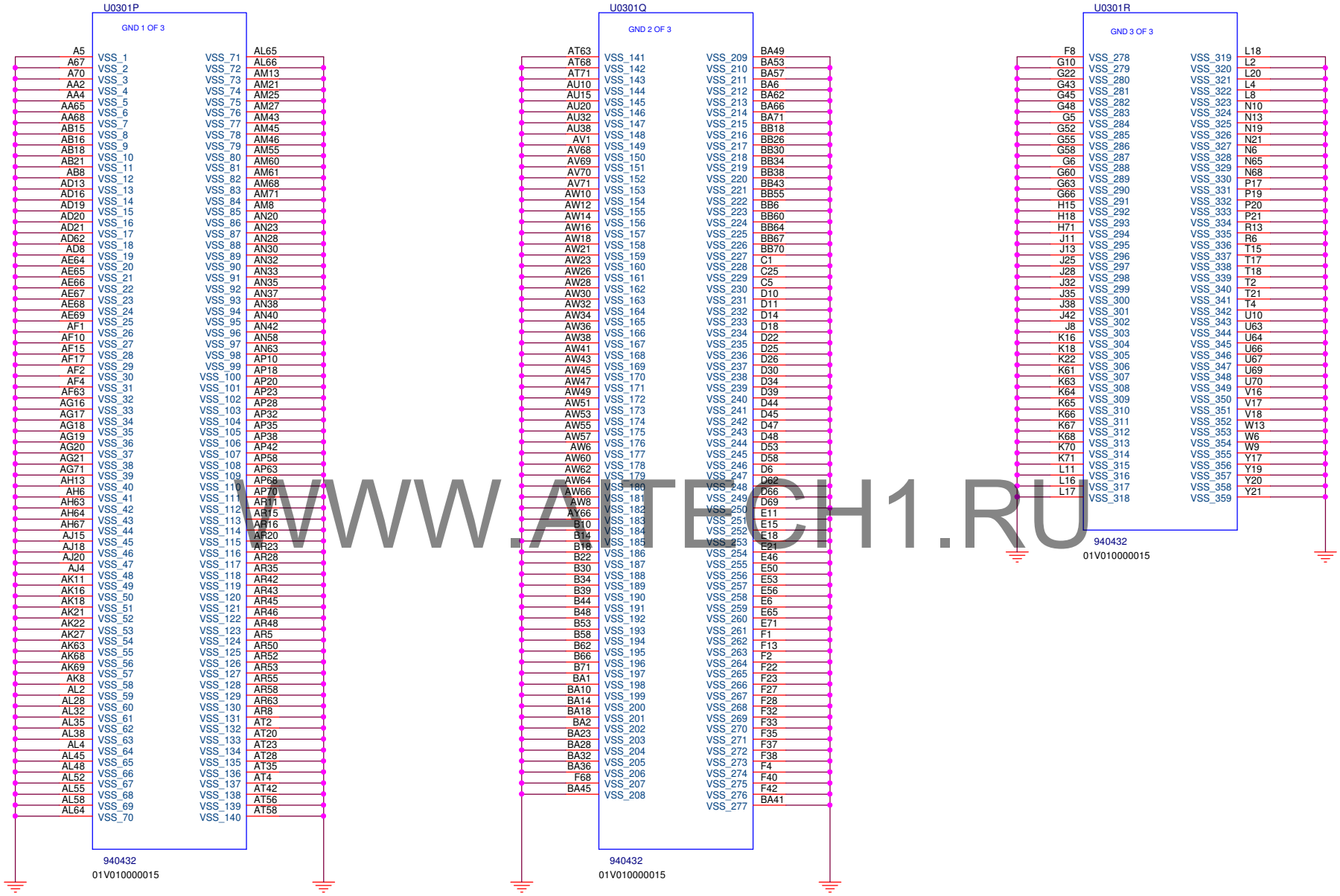
Title: CPU(5)_+VDDQ/IO/SA
BG1/HW3
Engineer: Bill Yang
Size: Custom
Project Name: AQ5EB
Rev: 1.0
Date: Wednesday, August 23, 2017
Sheet 7 of 108



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Title : CPU(6)_CPU GND

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BG1/HW3

Engineer: Bill Yang

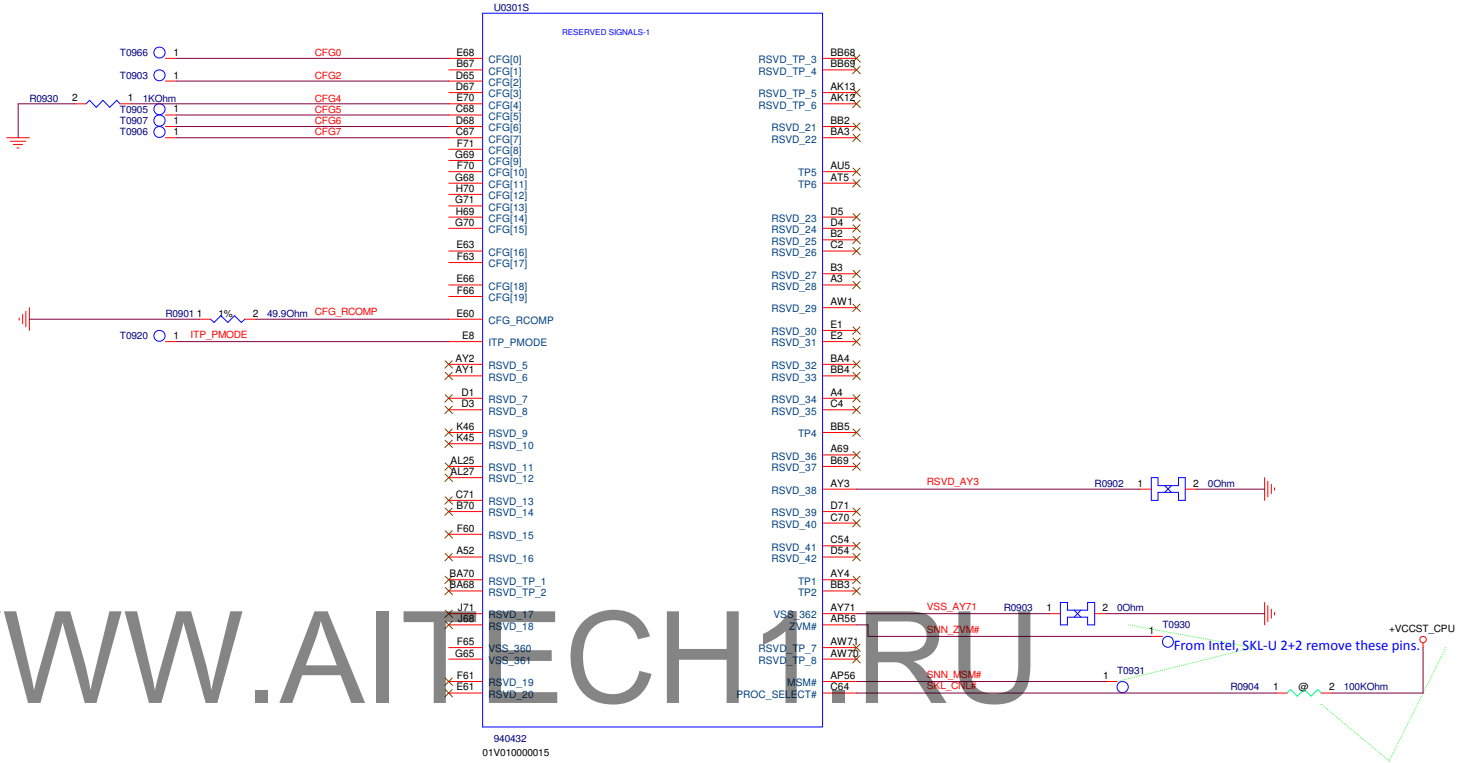
| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 1.0 |

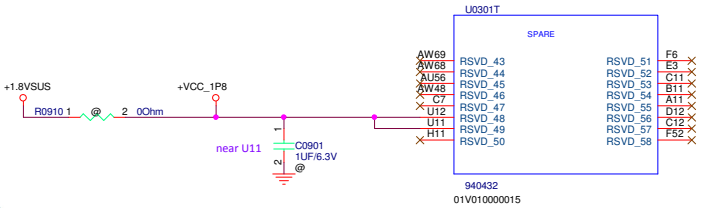
Date: Wednesday, August 23, 2017 Sheet 8 of 108

## 6.4 Reset and Miscellaneous Signals

**Table 6-8. Reset and Miscellaneous Signals**

| Signal Name | Description | Dir. | Buffer Type | Link Type | Availability |
|---|---|---|---|---|---|
| CFG[19:0] | **Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.<br>Intel recommends placing test points on the board for CFG pins.<br>• **CFG[0]:** Stall reset sequence after PCU PLL lock until de-asserted:<br>– 1 = (Default) Normal Operation; No stall.<br>– 0 = Stall.<br>• **CFG[1]:** Reserved configuration lane.<br>• **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal.<br>– 1 = Normal operation<br>– 0 = Lane numbers reversed.<br>• **CFG[3]:** Reserved configuration lane.<br>• **CFG[4]:** eDP enable:<br>– 1 = Disabled.<br>– 0 = Enabled.<br>• **CFG[6:5]:** PCI Express* Bifurcation<br>– 00 = 1 x8, 2 x4 PCI Express*<br>– 01 = reserved<br>– 10 = 2 x8 PCI Express*<br>– 11 = 1 x16 PCI Express*<br>• **CFG[7]:** PEG Training:<br>– 1 = (default) PEG Train immediately following RESET# de assertion.<br>– 0 = PEG Wait for BIOS for training.<br>• **CFG[19:8]:** Reserved configuration lanes. | I/O | GTL | SE | All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them. |




### 1.3.2 [U] Skylake-U and Cannonlake-U Compatibility Decoupling Requirement

Two reserve pins (U11 and U12) for 1.8V were added to Skylake-U PCH to support Cannonlake-U PCH compatibility. For Skylake-U, the following changes will be made to Table 52-8 in the Skylake U/Y Platform Design Guide (IBP#543016).

**Table 52-8 – Decoupling and Power Connection Requirement for Skylake-U PCH**

| Voltage Supply | Area | PCH Pins sharing power rail | Value | Size | Quantity | Placement type (R)onway / (E)dge | Place capacitor(s) near ball(s) |
|---|---|---|---|---|---|---|---|
| V1.8A | VccPGPPF | AF16 | - | - | - | - | - |
| | VccATS | AA1 | 1 uF | 0402 | 1 | E (<10 mm) | AA1 |
| | Vcc_1P8 | U11, U12 | 1 uF | 0402 | 1 | E (<10 mm) | U11, U12 (Note 1 & 5) |



+VCCST_CPU — +VCCST_CPU 3,5,7,25
+1.8VSUS — +1.8VSUS 21,24,26,84

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Title :CPU(7)_CFG/RSVD
BG1/HW3
Engineer: Bill Yang
Size: Custom | Project Name: AQ5EB | Rev: 1.0
Date: Wednesday, August 23, 2017 | Sheet 9 of 108

<Variant Name>

PEGATRON Title :



Engineer:

| Size | Project Name | Rev |
|---|---|---|
| A3 | | 1.1 |

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<Variant Name>

PEGATRON Title :



Engineer:

| Size | Project Name | Rev |
|---|---|---|
| A3 | | 1.1 |

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| | | |
|---|---|---|
| Title <Title> | | |
| Size A | Document Number <Doc> | Rev <RevCode> |
| Date: Wednesday, August 23, 2017 | Sheet 12 of 108 | |

| | | |
|---|---|---|
| Title | <Title> | |
| Size A | Document Number <Doc> | Rev <RevCode> |
| Date: Wednesday, August 23, 2017 | Sheet 13 of 108 | |

<Variant Name>

PEGATRON Title :



Engineer:

| Size | Project Name | Rev |
|---|---|---|
| A3 | | 1.1 |

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# DDR4(0)_Termination

+0.6VS → +0.6VS 17,57,83

+1.2V → +1.2V 4,7,16,17,18,57,83

+0.6VS

| | | | | |
|---|---|---|---|---|
| 1 | 34.8Ohm 2 | R1501 1% /OBM | M0_MA0 | M_A_A0 4,16 |
| 1 | 34.8Ohm 2 | R1502 1% /OBM | M0_MA1 | M_A_A1 4,16 |
| 1 | 34.8Ohm 2 | R1503 1% /OBM | M0_MA2 | M_A_A2 4,16 |
| 1 | 34.8Ohm 2 | R1504 1% /OBM | M0_MA3 | M_A_A3 4,16 |
| 1 | 34.8Ohm 2 | R1505 1% /OBM | M0_MA4 | M_A_A4 4,16 |
| 1 | 34.8Ohm 2 | R1506 1% /OBM | M0_MA5 | M_A_A5 4,16 |
| 1 | 34.8Ohm 2 | R1507 1% /OBM | M0_MA6 | M_A_A6 4,16 |
| 1 | 34.8Ohm 2 | R1508 1% /OBM | M0_MA7 | M_A_A7 4,16 |
| 1 | 34.8Ohm 2 | R1509 1% /OBM | M0_MA8 | M_A_A8 4,16 |
| 1 | 34.8Ohm 2 | R1510 1% /OBM | M0_MA9 | M_A_A9 4,16 |
| 1 | 34.8Ohm 2 | R1511 1% /OBM | M_A_A10_AP | M_A_A10 4,16 |
| 1 | 34.8Ohm 2 | R1512 1% /OBM | M0_MA11 | M_A_A11 4,16 |
| 1 | 34.8Ohm 2 | R1513 1% /OBM | M0_MA12 | M_A_A12 4,16 |
| 1 | 34.8Ohm 2 | R1514 1% /OBM | M0_MA13 | M_A_A13 4,16 |
| 1 | 34.8Ohm 2 | R1515 1% /OBM | M_A_A14_WE_N | M_A_A14 4,16 |
| 1 | 34.8Ohm 2 | R1516 1% /OBM | M_A_A15_CAS_N | M_A_A15 4,16 |
| 1 | 34.8Ohm 2 | R1529 1% /OBM | M_A_A16_RAS_N | M_A_A16 4,16 |

+0.6VS

| | | | |
|---|---|---|---|
| 4,16 | M_A_DIM0_CS#0 | 1% R1521 1 /OBM 2 | 34.8Ohm |
| 4,16 | M_A_DIM0_CKE0 | 1% R1522 1 /OBM 2 | 34.8Ohm |

+0.6VS

| | | | |
|---|---|---|---|
| 4,16 | M_A_BG0 | 1% R1523 2 /OBM 1 | 34.8Ohm |
| 4,16 | M_A_BG1 | 1% R1538 2 /DDP 1 | 34.8Ohm |
| 4,16 | M_A_BA0 | 1% R1524 2 /OBM 1 | 34.8Ohm |
| 4,16 | M_A_BA1 | 1% R1525 2 /OBM 1 | 34.8Ohm |
| 4,16 | M_A_DIM0_ODT0 | 1% R1530 2 /OBM 1 | 34.8Ohm |
| 4,16 | M_A_ACT# | 1% R1532 2 /OBM 1 | 34.8Ohm |
| 4,16 | M_A_PAR | 1% R1534 2 /OBM 1 | 34.8Ohm |

+0.6VS

| | | | |
|---|---|---|---|
| 4,16 | M_A_DIM0_CLK#0 | vx_r0402_small 5% R1536 1 /OBM 2 | 36Ohm |
| 4,16 | M_A_DIM0_CLK0 | vx_r0402_small 5% R1537 1 /OBM 2 | 36Ohm |

+1.2V

| | | | |
|---|---|---|---|
| 4,16 | M_A_ALERT# | vx_r0402_small 1% R1535 1 /OBM 2 | 49.9Ohm |

Average placed close to +VDDQ_VTT power plane

+0.6VS

| | | |
|---|---|---|
| C1501 | 1UF/6.3V /OBM | vx_c0402_small |
| C1502 | 1UF/6.3V /OBM | vx_c0402_small |
| C1053 | 1UF/6.3V /OBM | vx_c0402_small |
| C1504 | 1UF/6.3V /OBM | vx_c0402_small |
| C1505 | 1UF/6.3V /OBM | vx_c0402_small |
| C1506 | 1UF/6.3V /OBM | vx_c0402_small |
| C1507 | 1UF/6.3V /OBM | vx_c0402_small |
| C1508 | 1UF/6.3V /OBM | vx_c0402_small |

+0.6VS

| | | |
|---|---|---|
| C1509 | 10UF/6.3V /OBM | |
| C1510 | 10UF/6.3V /OBM | |



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Title : DDR4(1)_Termination

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BG1-NB4

Engineer: Bill Yang

| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 1.0 |

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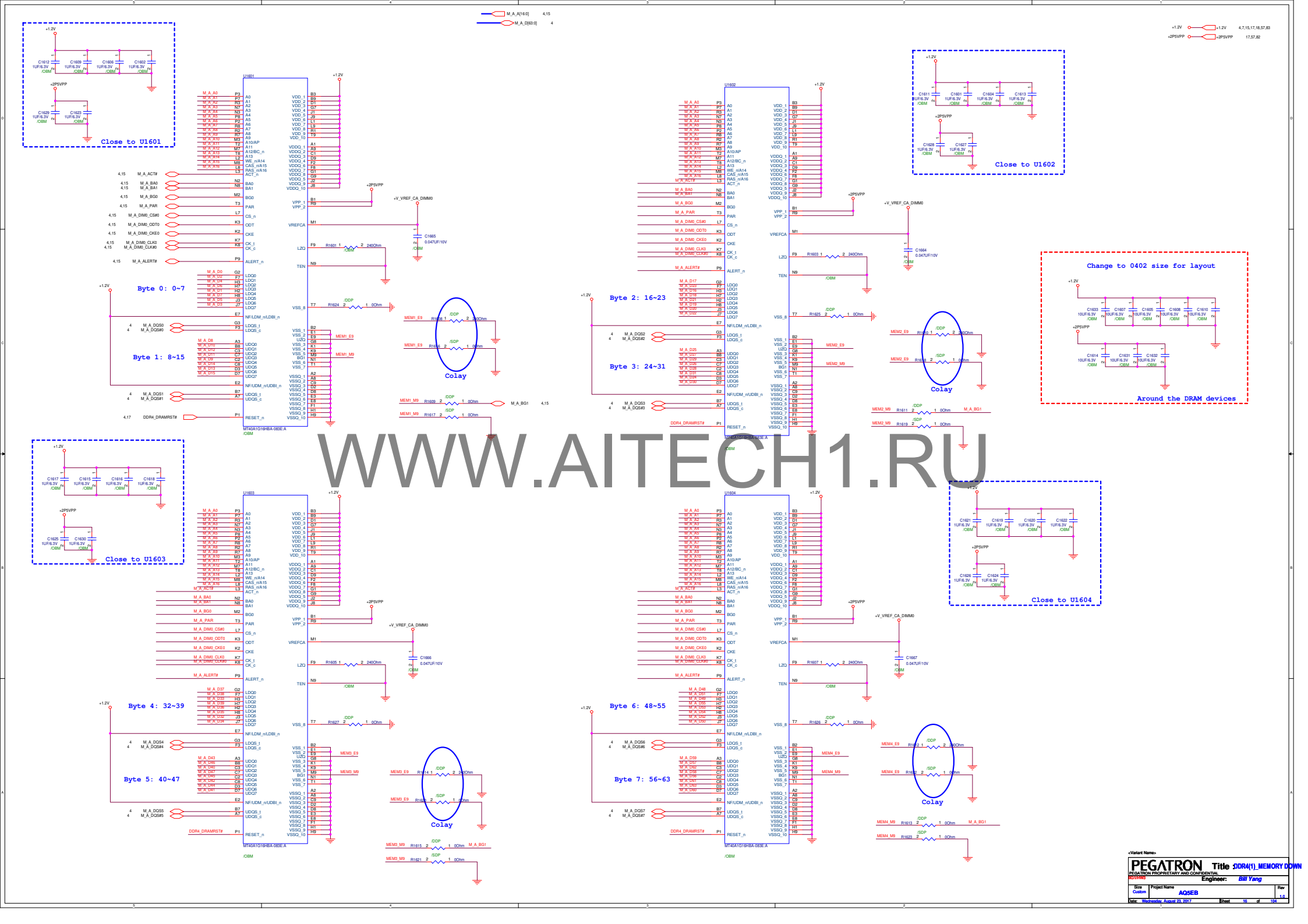

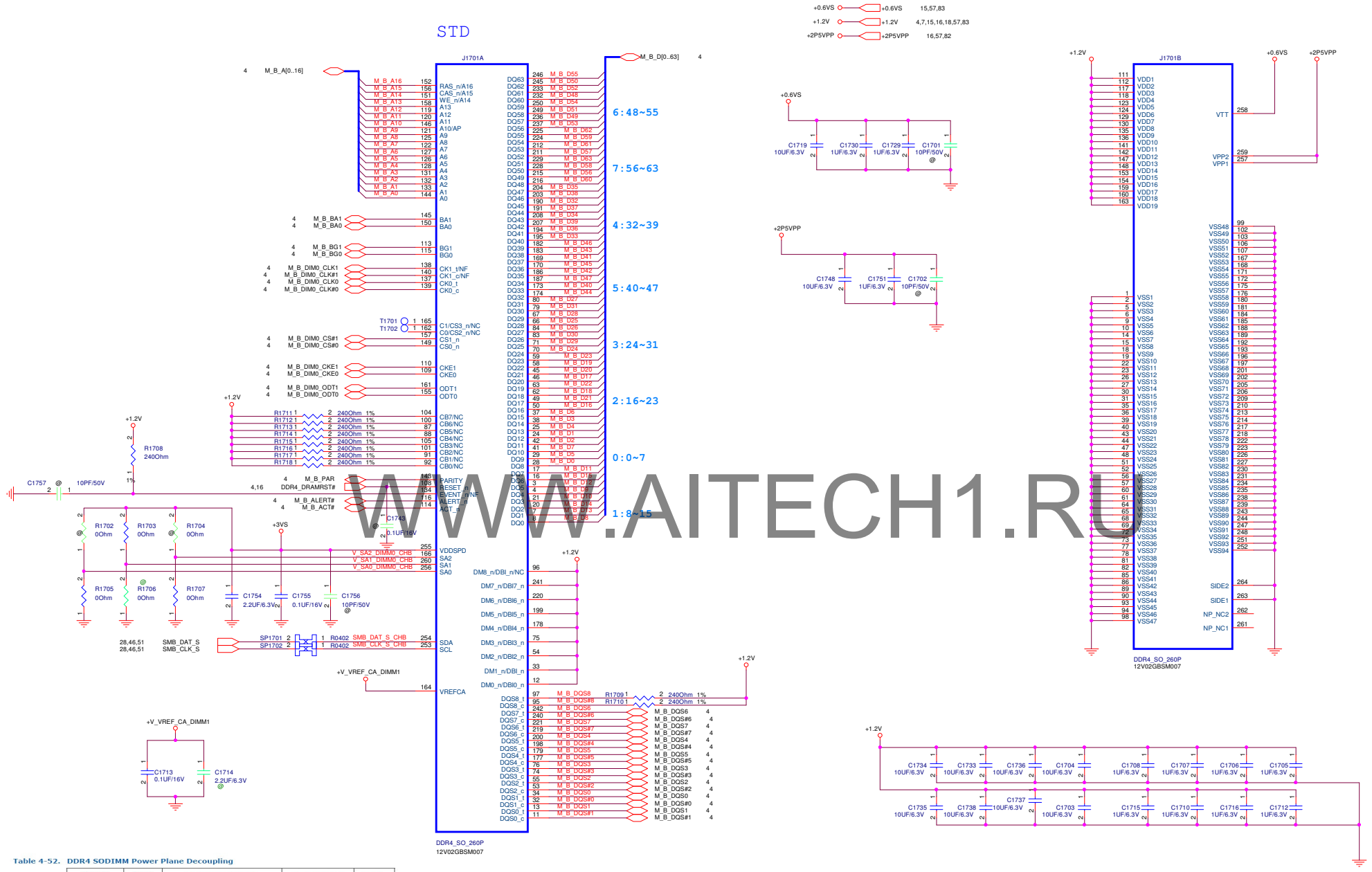




Table 4-52. DDR4 SODIMM Power Plane Decoupling

| Memory Configuration | Power Domain | Decoupling Location | Qty x µF (size) | Note |
|---|---|---|---|---|
| DDR4 SODIMM 1DPC | VDDQ | 4 near each side of the DIMM connector close to VDD pins | 16x 10µF (0603) | |
| | | 4 near each side of the DIMM connector close to VDD pins | 16x 1µF (0402) | |
| | | 1 placeholder | 1x 330µF (7343) | |
| | VTT | Place these caps on the VTT plane close to SODIMM | 1x 10µF (0805) | |
| | | Placeholder<br>Place these caps on the VTT plane close to SODIMM | 1x 10µF (0805) | |
| | | Place these caps on the VTT plane close to SODIMM | 4x 1µF (0402) | |
| | VPP | DRAM Side | 2x 10µF (0603) | |
| | | DRAM Side | 2x 1µF (0402) | |
| | VDDSPD | Place close to DIMM | 1x 0.1µF (0402) | |
| | | Place close to DIMM | 1x 2.2µF (0402) | |

*Notes:*
1. Total quantity is referring to 2 channels.

<Variant Name>

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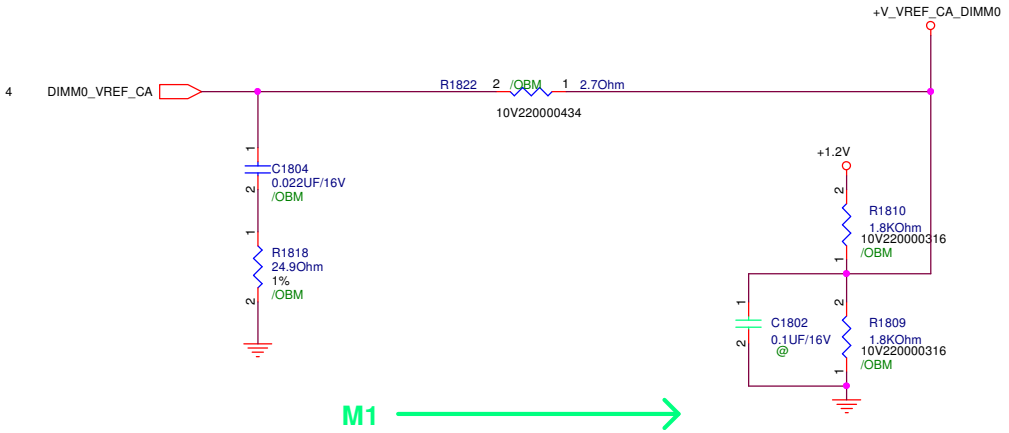
Title : DDR4(1)_SO-DIMM
BG1/HW3
Engineer: Bill Yang
Size: Custom | Project Name: AQ5EB | Rev: 1.0
Date: Wednesday, August 23, 2017 | Sheet 17 of 108

M3: CPU driven VREF path is stuffed be default.
M1: VREF_DQ driven by a Voltage Divider Network during Processor power-off

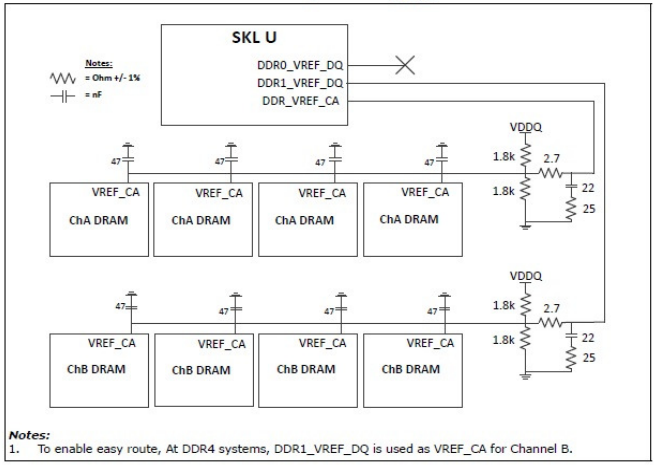
+1.2V — +1.2V — 4,7,15,16,17,57,83
+V_VREF_CA_DIMM0 — +V_VREF_CA_DIMM0 — 16
+V_VREF_CA_DIMM1 — +V_VREF_CA_DIMM1 — 17

M3 →




M1 →

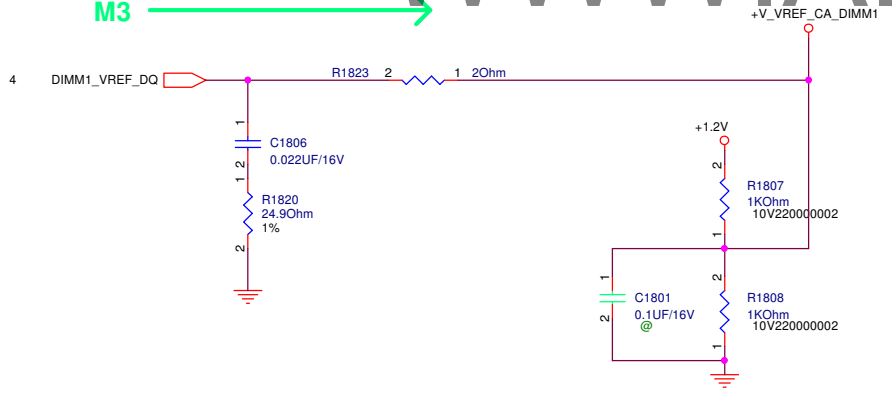
Figure 4-46. SKL U DDR4/-RS x16 Devices Memory Down $V_{REF-CA}$ Overview




*Notes:*
1. To enable easy route, At DDR4 systems, DDR1_VREF_DQ is used as VREF_CA for Channel B.

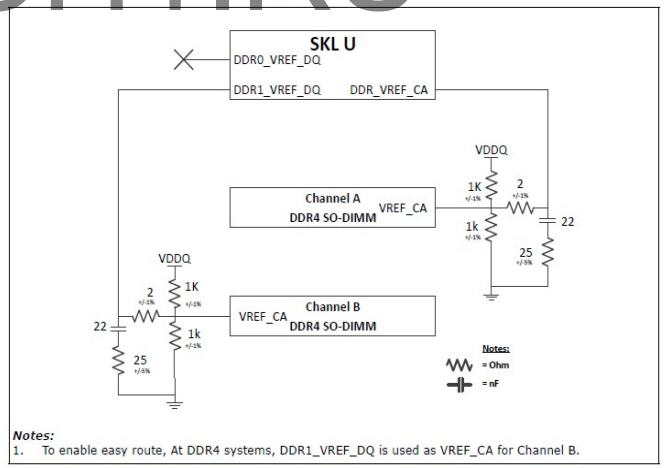


M3 →




M1 →

Figure 4-45. SKL U DDR4/-RS SODIMM $V_{REF-CA}$ Overview




*Notes:*
1. To enable easy route, At DDR4 systems, DDR1_VREF_DQ is used as VREF_CA for Channel B.

<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : DDR4(3)_CA/DQ Voltag
Engineer: Bill Yang
BG1/HW3
Size: Custom | Project Name: AQ5EB | Rev: 1.0
Date: Wednesday, August 23, 2017 | Sheet 18 of 108

<Variant Name>

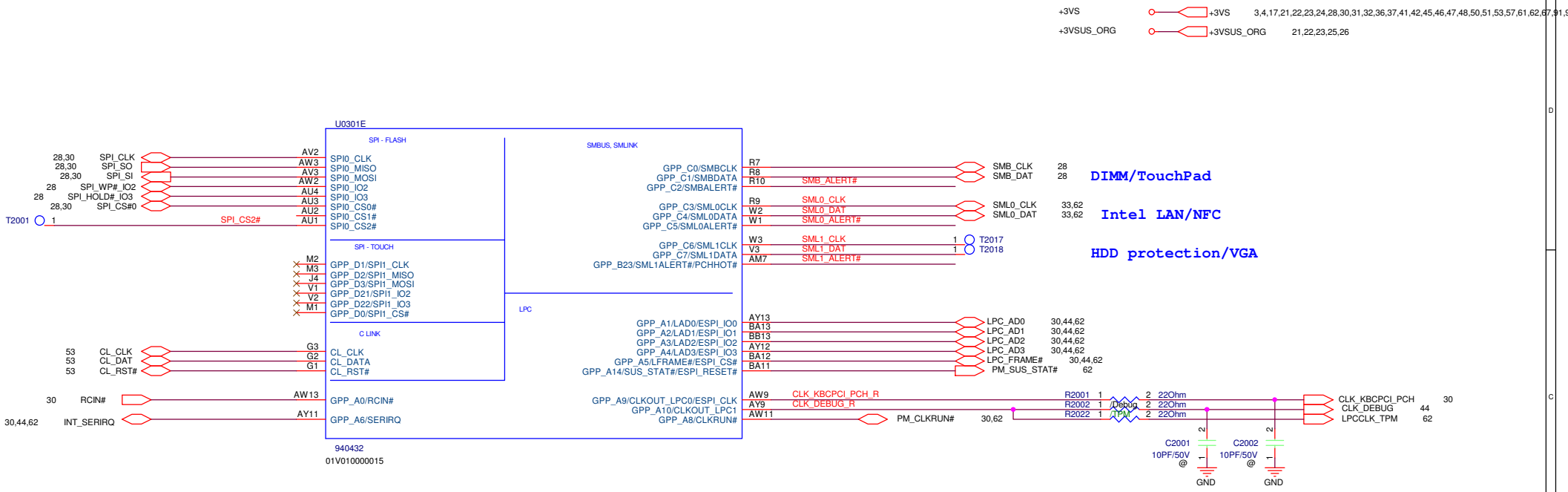
PEGATRON Title :



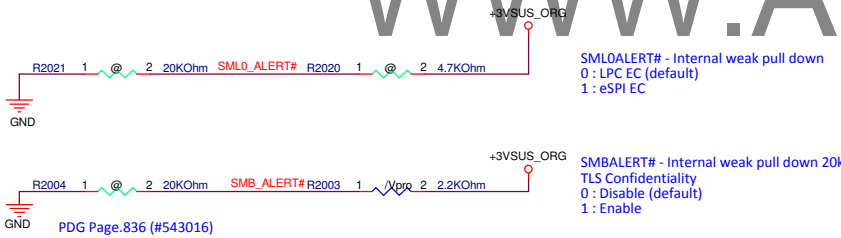
Engineer:

| Size | Project Name | Rev |
|---|---|---|
| A3 | | 1.1 |

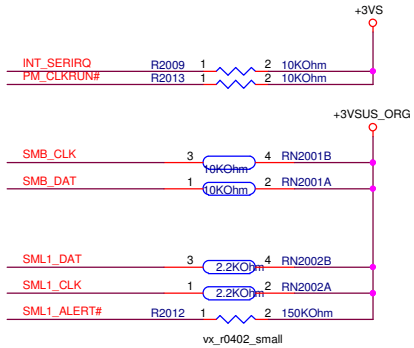
Date: Wednesday, August 23, 2017 Sheet 19 of 108






| | | | |
|---|---|---|---|
| **SMBALERT# / GPP_C2** | TLS Confi-dentiality | Rising edge of RSMRST# | This signal has a weak internal pull-down.<br>0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)<br>1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.<br>***Notes:***<br>1. The internal pull-down is disabled after RSMRST# de-asserts.<br>2. This signal is in the primary well. |




<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

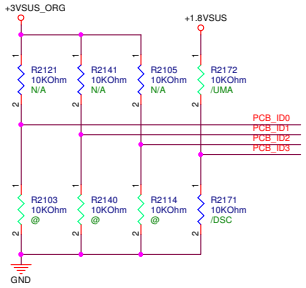
Title : PCH(1)_SMB,LPC

Engineer: Bill Yang

BG1/HW3

| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 1.0 |

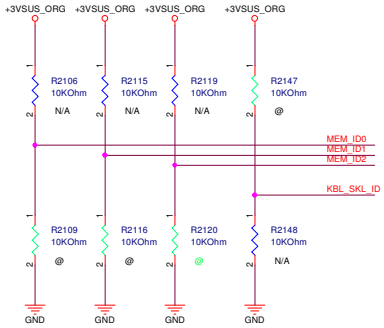
Date: Wednesday, August 23, 2017 Sheet 20 of 108

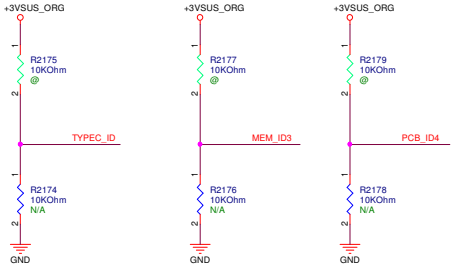


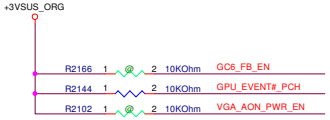

| ID2 | ID1 | ID0 | PCB Rev. |
|---|---|---|---|
| 0 | 0 | 0 | R1.0 |
| 0 | 0 | 1 | R1.1 |
| 0 | 1 | 0 | R2.0 |
| 0 | 1 | 1 | R2.1 |
| 1 | 0 | 0 | TBD |
| 1 | 0 | 1 | TBD |
| 1 | 1 | 0 | TBD |
| 1 | 1 | 1 | P2 |

| MEM_ID0 | MEM_ID1 | MEM_ID2 | Memory Setting |
|---|---|---|---|
| 0 | 0 | 0 | ~~SAMSUNG/K4A4G165WD-BCPB 4Gb 256Mb*16 0315-01C70PB~~ |
| 1 | 0 | 0 | HYNIX/H5ANAG6NAMR-UHC 0315-02640PB HYNIX DDP 8G |
| 0 | 1 | 0 | SAMSUNG/K4A8G165WB-BCPB 8Gb 512Mb*16 0315-01HF0PB |
| 1 | 1 | 0 | DR4 2400 1Gb*16 1.2V FBGA96 MICRON/MT40A1G16WBU-083E:B 0315-01YC0PB NEW Micron DDP for 8L |
| 0 | 0 | 1 | SAMSUNG/K4A8G165WB-BCRC 2400 512Mb*16 0315-01C80PB |
| 1 | 0 | 1 | SK HYNIX/H5AN8G6NAFR-UHC 2400 512Mb*16 0315-01W60PB |
| 0 | 1 | 1 | MICRON/MT40A512M16JY-083E:B 2400 512Mb*16 0315-01W90PB |
| 1 | 1 | 1 | DR4 2400 1Gb*16 1.2V FBGA96 MICRON/MT40A1G16WBU-083E:B 0315-01YC0PB old Micron DDP for 6L |


| KBL_SKL_ID | SSD_PRSENT# | NFC_ID | PCB_ID3 | TYPEC_ID |
|---|---|---|---|---|
| 1:SKL | 1: No SSD | 1: No NFC | 1: UMA | 1: RTS5440 |
| 0: KBL | 0: SSD | 0: NFC | 0: DSC | 0: ANX7428 |

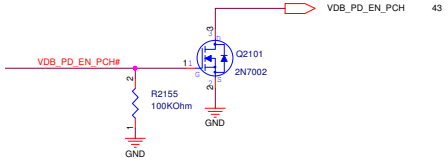


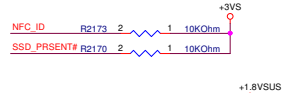



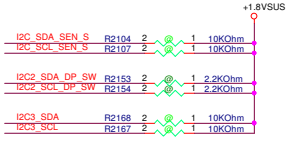



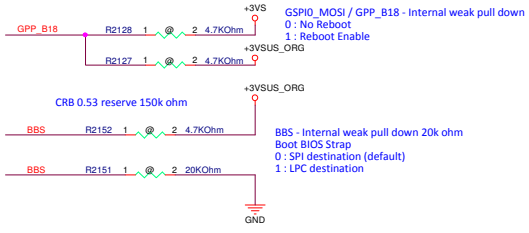

GPIO need to pull high to power with 10Kohm if unused

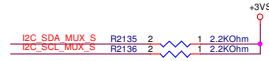





<Variant Name>

PEGATRON Title : PCH(2) LPSS,ISH

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Bill Yang

BG1/HW3

| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 1.0 |

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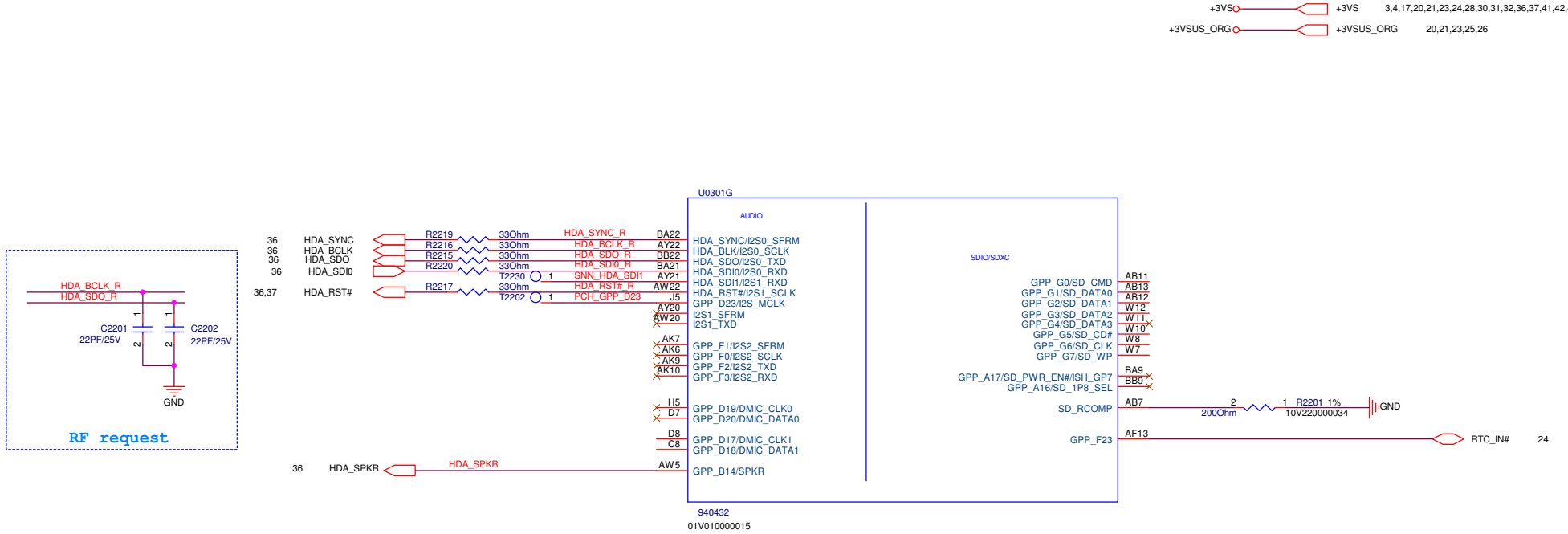





<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

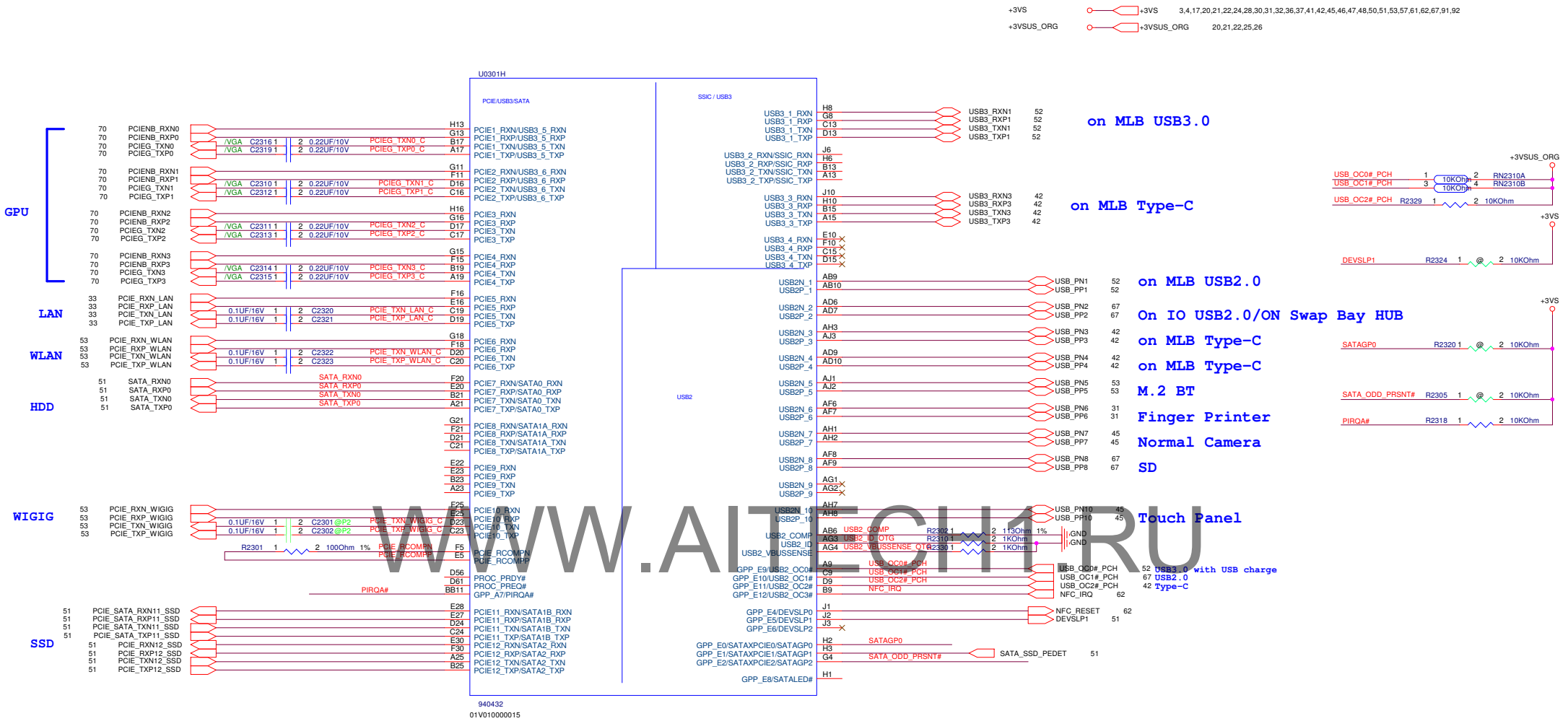
Title : PCH(3),HDA,SDIO

Engineer: Bill Yang

BG1/HW3

| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 1.0 |

Date: Wednesday, August 23, 2017 Sheet 22 of 108






### 3.4.1 SKL PCH U Flexible I/O

**Table 1-2. PCH-LP SKUs (Sheet 2 of 2)**

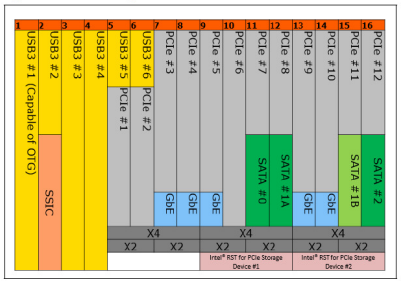
| Features | Base-U | Premium-U | Premium-Y |
|---|---|---|---|
| Total Intel® RST capable PCIe and SATA Express[4] Storage Devices | 0 | 2 | 2 |

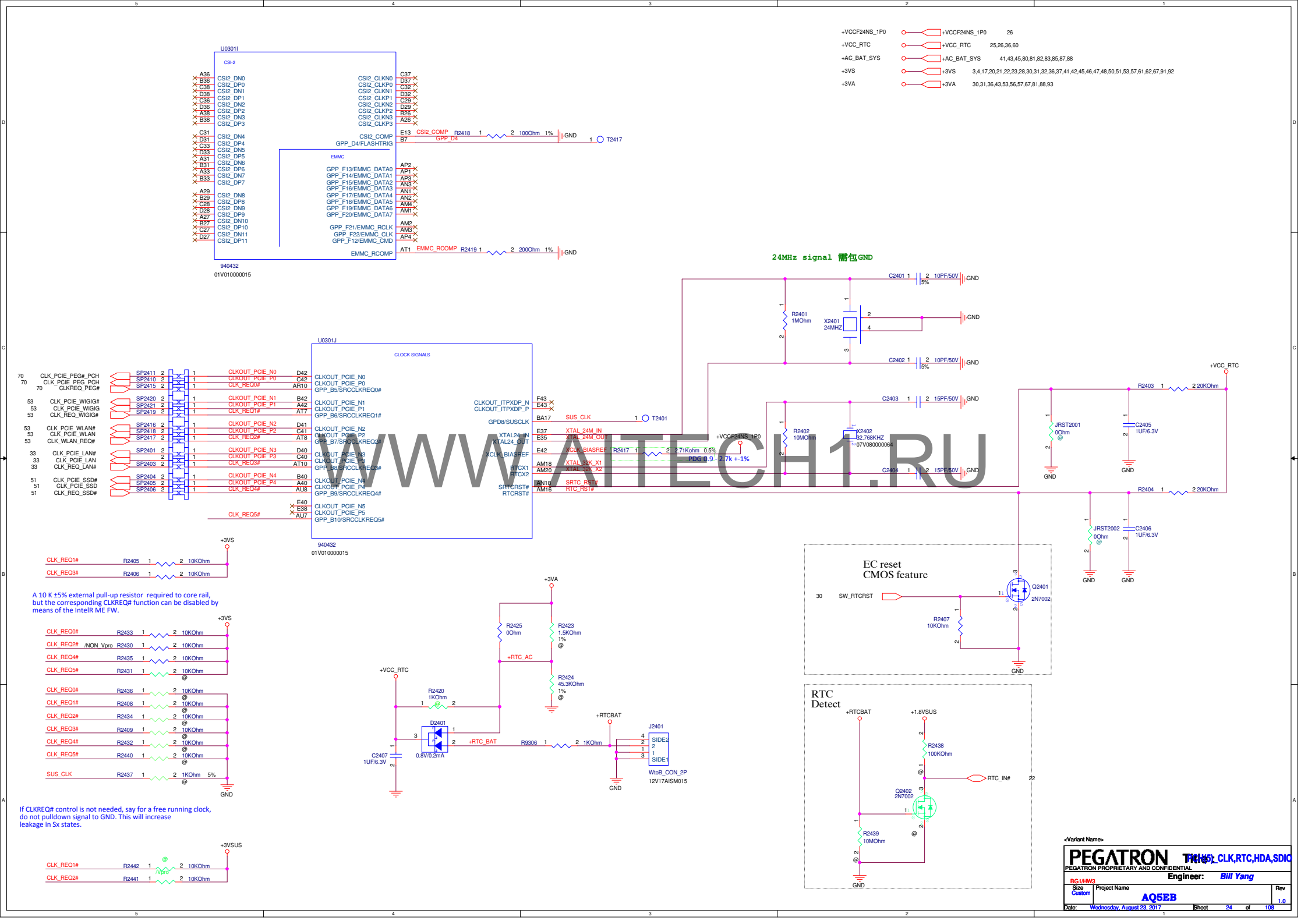
**Notes:**
1. USB 2.0 port numbers: 1-8
2. USB 2.0 port numbers: 1-10
3. USB 2.0 port numbers: 1-6
4. SATA Express Capable Ports (x2)

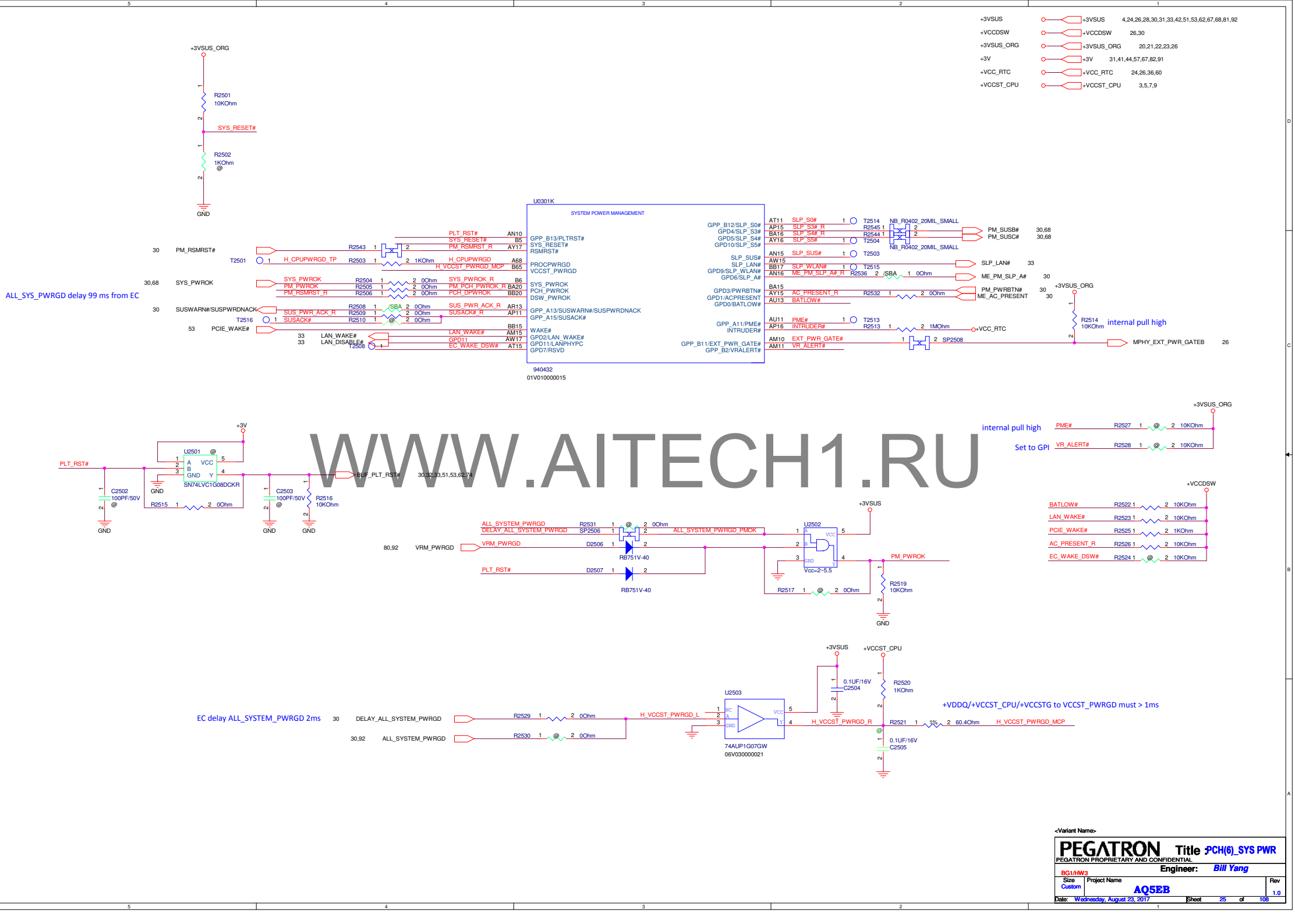
**Table 1-3. PCH-LP HSIO Detail**

| SKU | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Base-U | USB 3.0/ OTG | USB 3.0/ SSIC | USB 3.0 | USB 3.0 | PCIe | PCIe | PCIe/ LAN | PCIe/ LAN | PCIe/ LAN | PCIe | SATA | SATA | PCIe/ LAN | PCIe/ LAN | N/A | N/A |
| Premium-U | USB 3.0/ OTG | USB 3.0/ SSIC | USB 3.0 | USB 3.0 | PCIe/ USB 3.0 | PCIe/ USB 3.0 | PCIe/ LAN | PCIe/ LAN | PCIe/ LAN | PCIe | PCIe/ SATA | PCIe/ SATA | PCIe/ LAN | PCIe/ LAN | PCIe/ SATA | PCIe/ SATA |
| Premium-Y | USB 3.0/ OTG | USB 3.0/ SSIC | USB 3.0 | USB 3.0 | PCIe/ USB 3.0 | PCIe/ USB 3.0 | PCIe/ LAN | PCIe/ LAN | PCIe/ LAN | PCIe | PCIe/ SATA | PCIe/ SATA | PCIe/ LAN | PCIe/ LAN | N/A | N/A |

**Figure 3-1. HSIO Muxing on SKL PCH U**








<Variant Name>

PEGATRON PROPRIETARY AND CONFIDENTIAL

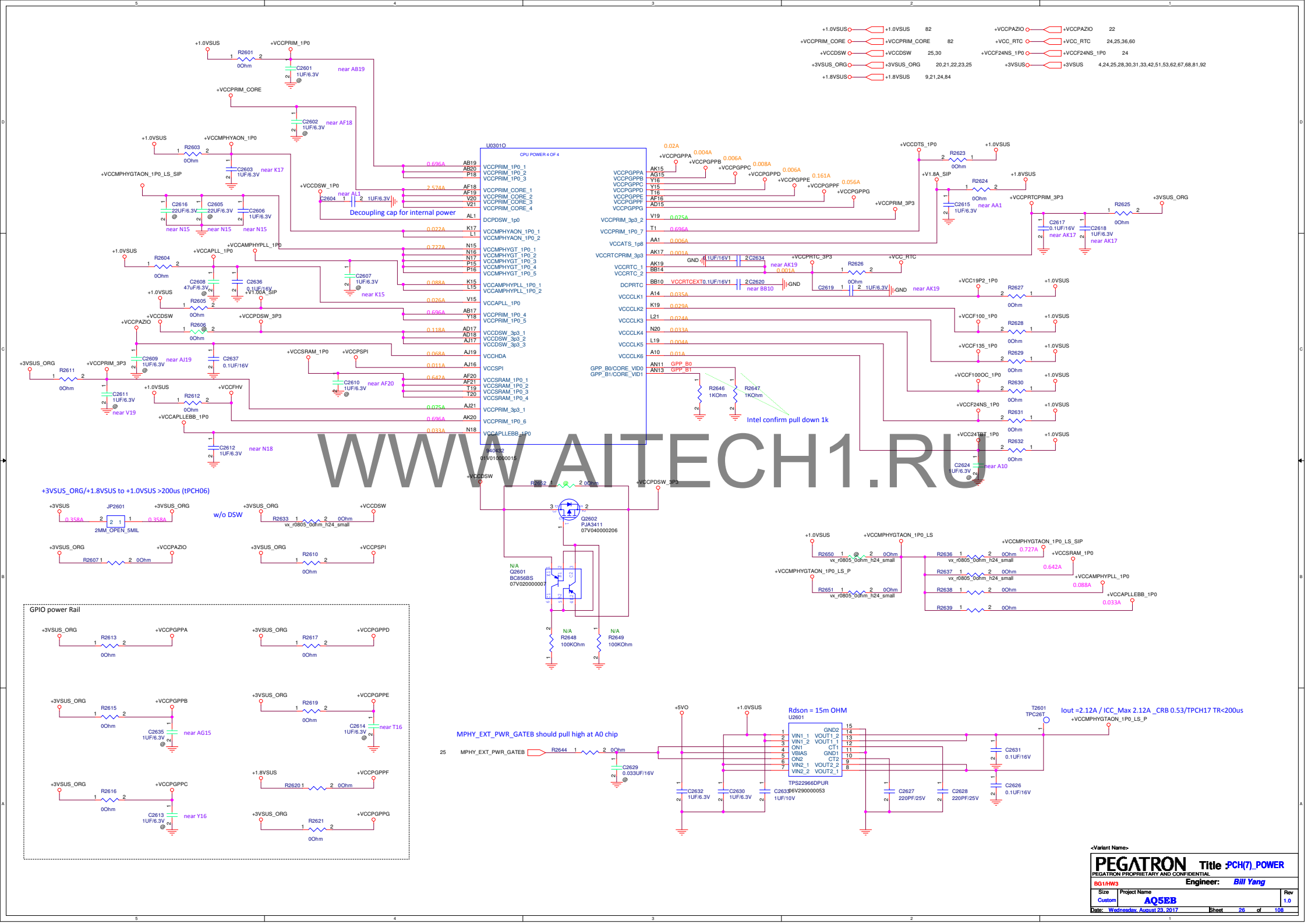
Title : PCH(6)_SYS PWR

Engineer: Bill Yang

BG1/HW3

Size: Custom | Project Name: AQ5EB | Rev: 1.0

Date: Wednesday, August 23, 2017 | Sheet 25 of 108






<Variant Name>

PEGATRON Title :PCH(7)_POWER

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3 Engineer: Bill Yang

| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 1.0 |

Date: Wednesday, August 23, 2017 Sheet 26 of 108

<Variant Name>

PEGATRON Title :

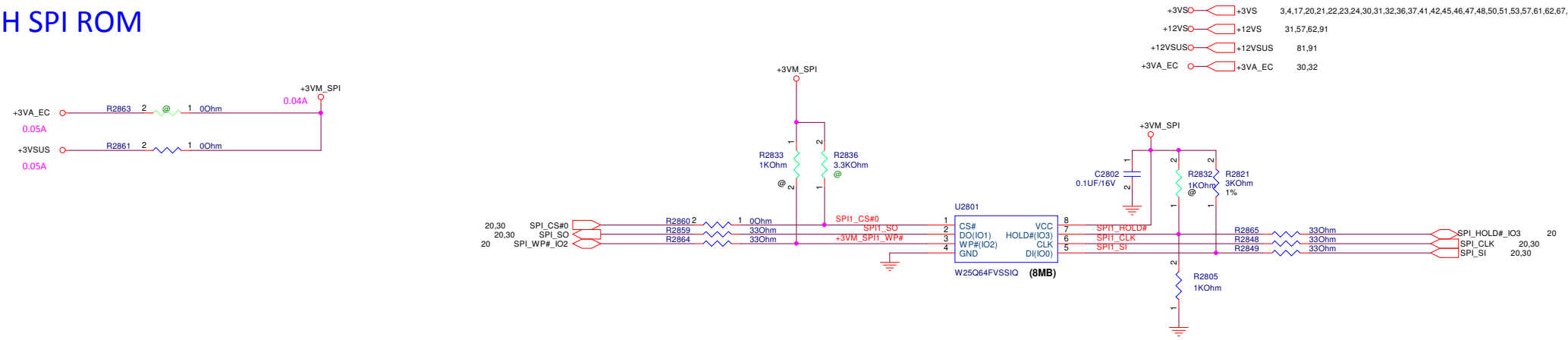


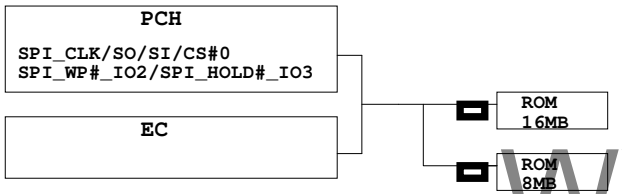
Engineer:

| Size | Project Name | Rev |
|---|---|---|
| A3 | | 1.1 |

Date: Wednesday, August 23, 2017 Sheet 27 of 108

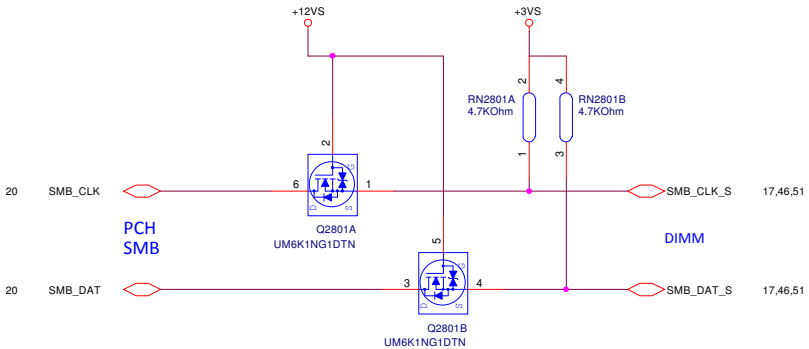
# PCH SPI ROM






# PCH SMBus




PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1/HW3

Title: PCH(8)_SPI,SMB
Engineer: Bill Yang
Size: Custom
Project Name: AQ5EB
Rev: 1.0
Date: Wednesday, August 23, 2017
Sheet 28 of 108

<Variant Name>

PEGATRON Title :

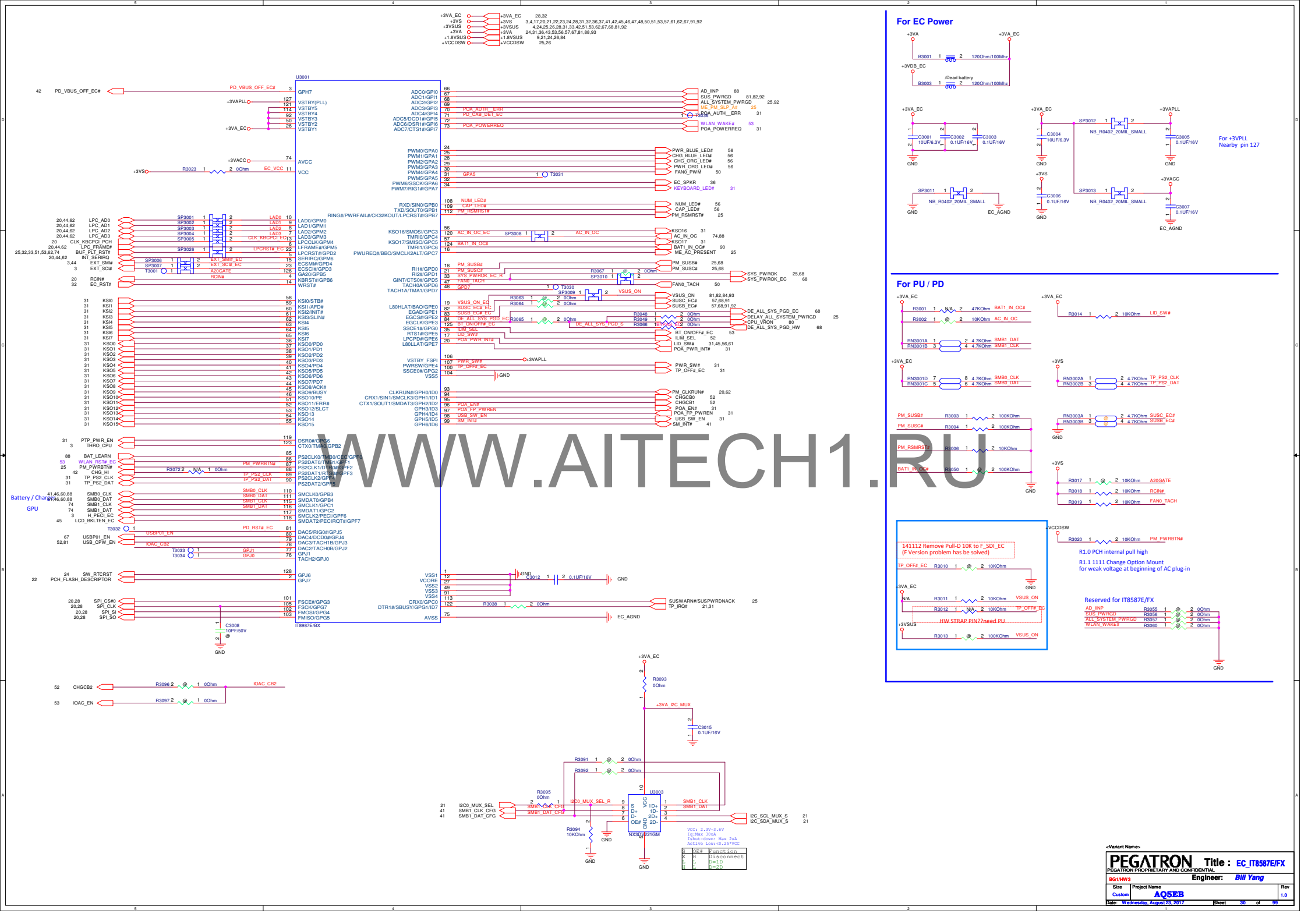
PEGATRON PROPRIETARY AND CONFIDENTIAL

<Title>

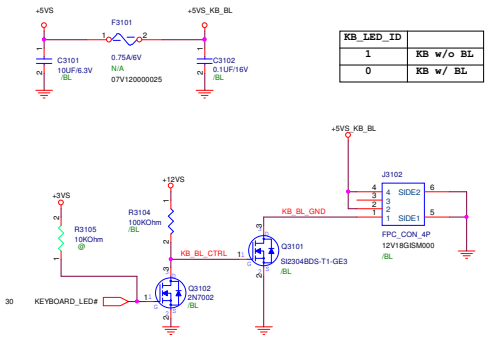
Engineer:

| Size | Project Name | Rev |
|---|---|---|
| C | AQ5EB | 1.1 |

Date: Wednesday, August 23, 2017 Sheet 29 of 108

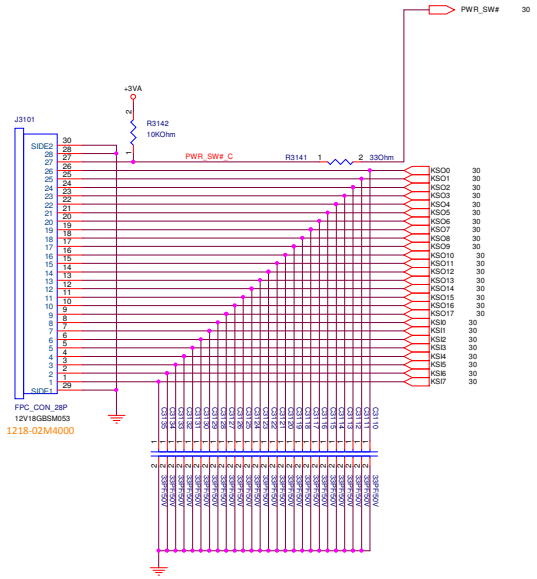


## Keyboard LED

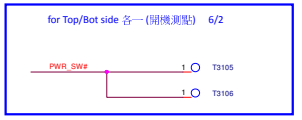


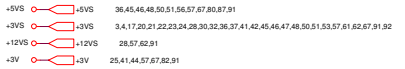

| KB_LED_ID | |
|---|---|
| 1 | KB w/o BL |
| 0 | KB w/ BL |

## Keyboard

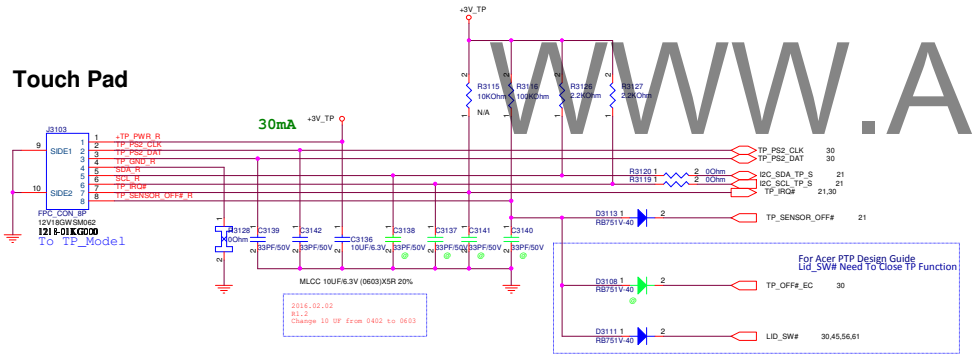



for Top/Bot side 各一(開機測點) 6/2

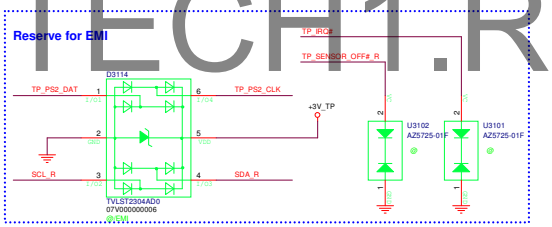


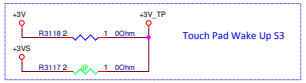



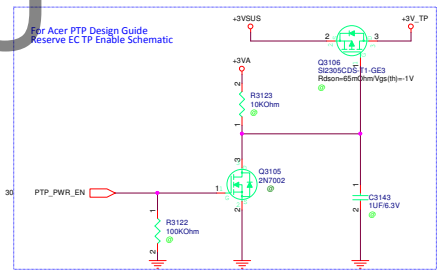

## Touch Pad



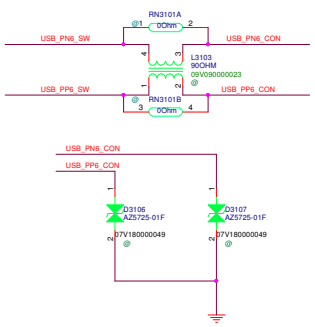

Reserve for EMI

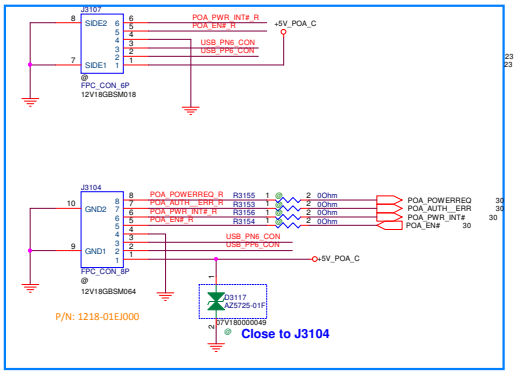


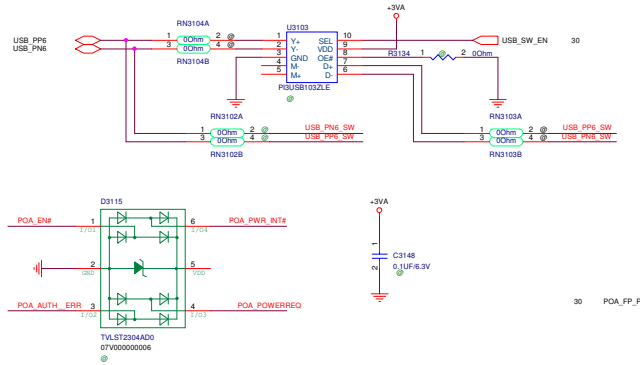



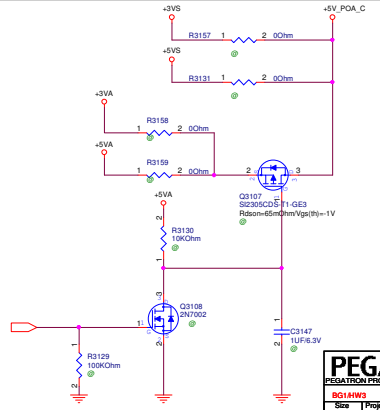

## Finger Print




J3107.1 and J3104.1 colay




PEGATRON Title : TP / KB / FP

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW3 Engineer: Bill Yang

| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 1.0 |

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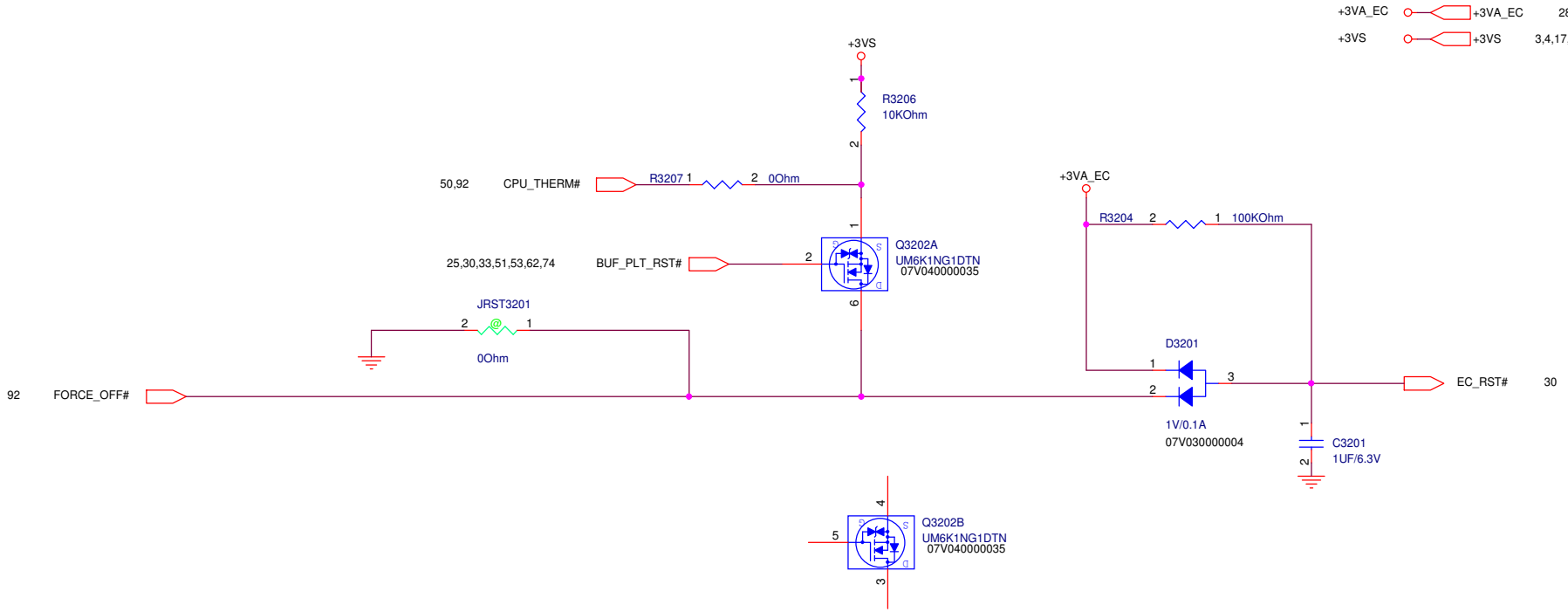





**Remove 10s RTC reset**

PEGATRON PROPRIETARY AND CONFIDENTIAL

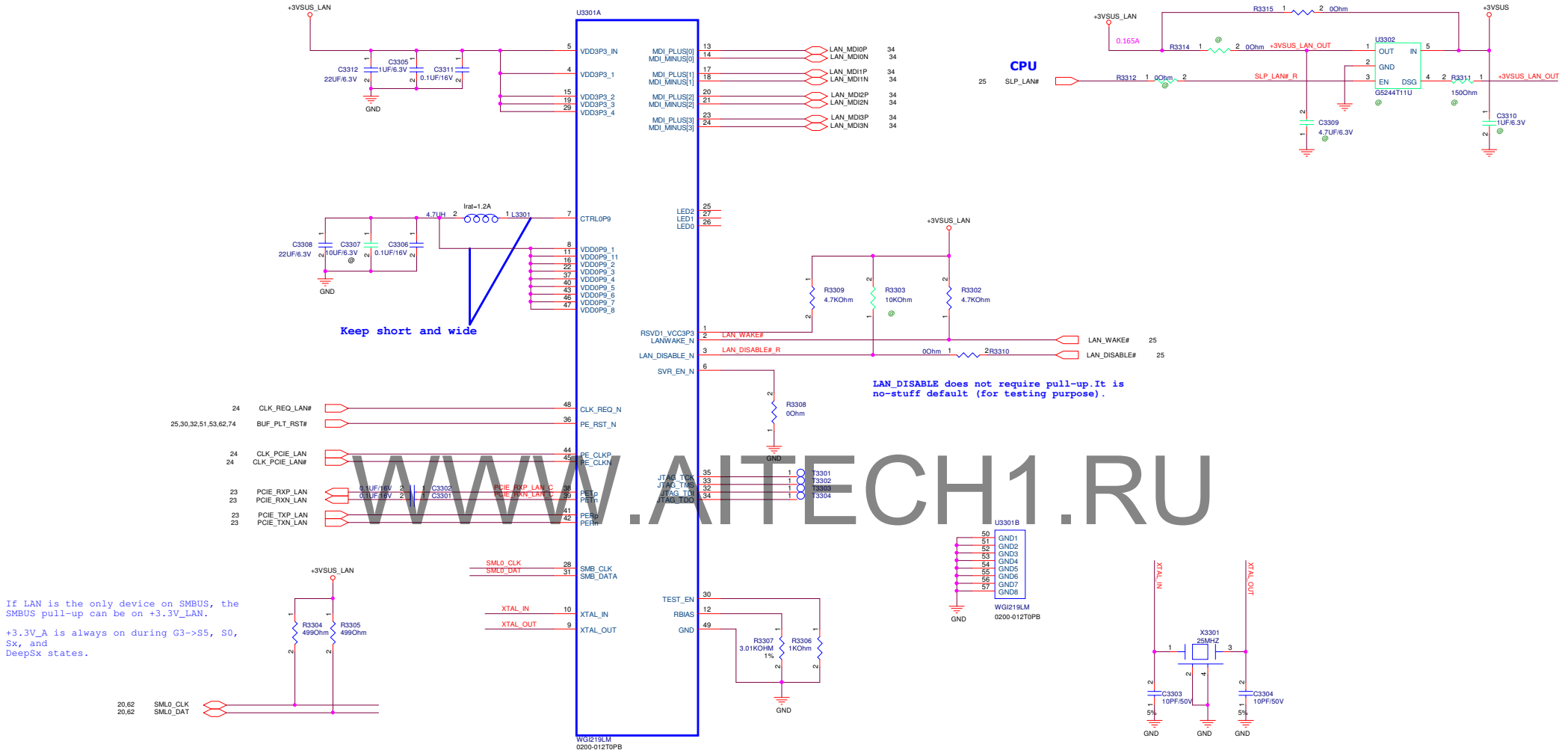
PEGATRON Title : RST_Reset Circuit

Engineer: Bill Yang

BG1/HW3

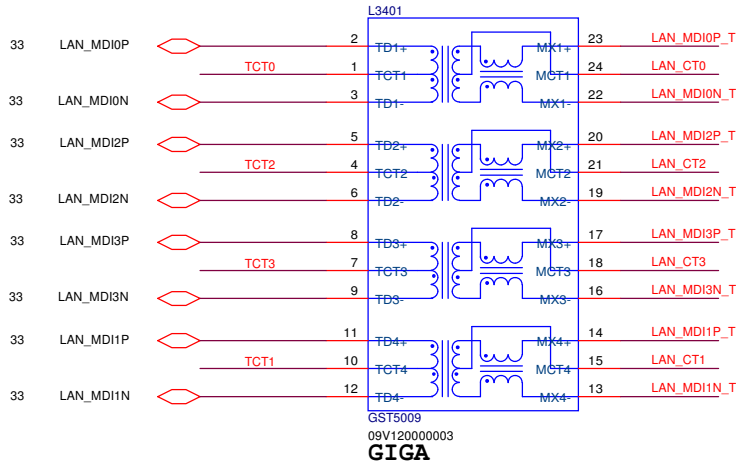
| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 1.0 |

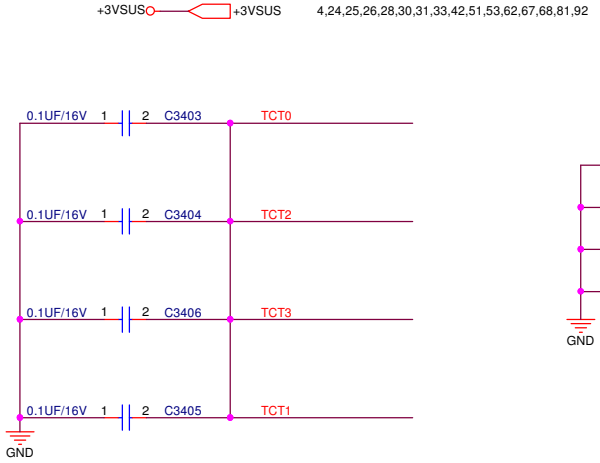
Date: Wednesday, August 23, 2017 Sheet 32 of 108

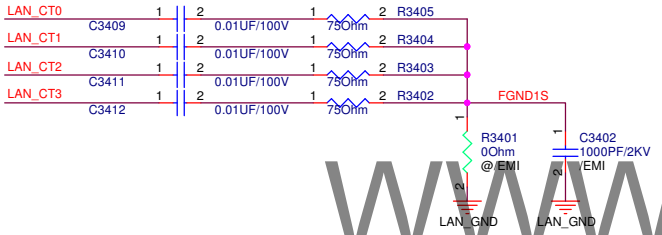


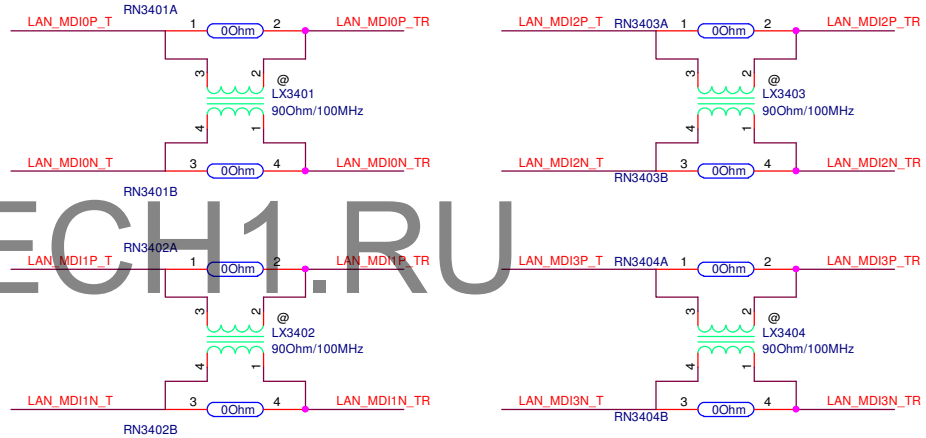


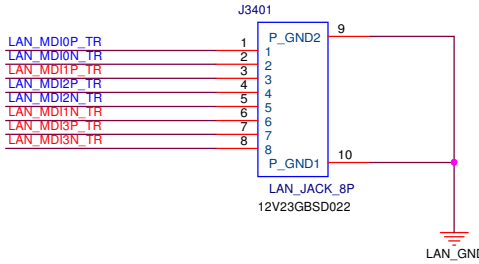

| | | | |
|---|---|---|---|
| PEGATRON | Title : | Intel/I219 | |
| BG1\HW3 | Engineer: | Bill Yang | |
| Size: Custom | Project Name: AQ5EB | | Rev: 1.0 |
| | P/N: | | |
| Date: Wednesday, August 23, 2017 | Sheet 33 of 108 | | |

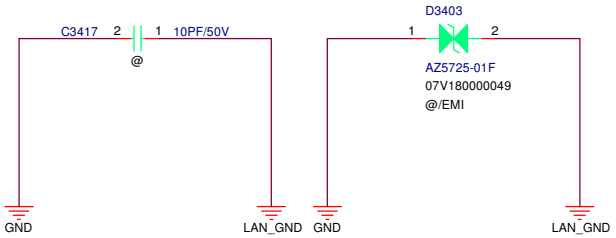


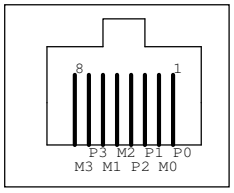




Place near chassis GND



PEGATRON

Title : RJ45

BG1\HW3

Engineer: Bill Yang

| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 1.0 |
| | P/N | |

Date: Wednesday, August 23, 2017 Sheet 34 of 108

<Variant Name>

PEGATRON Title :



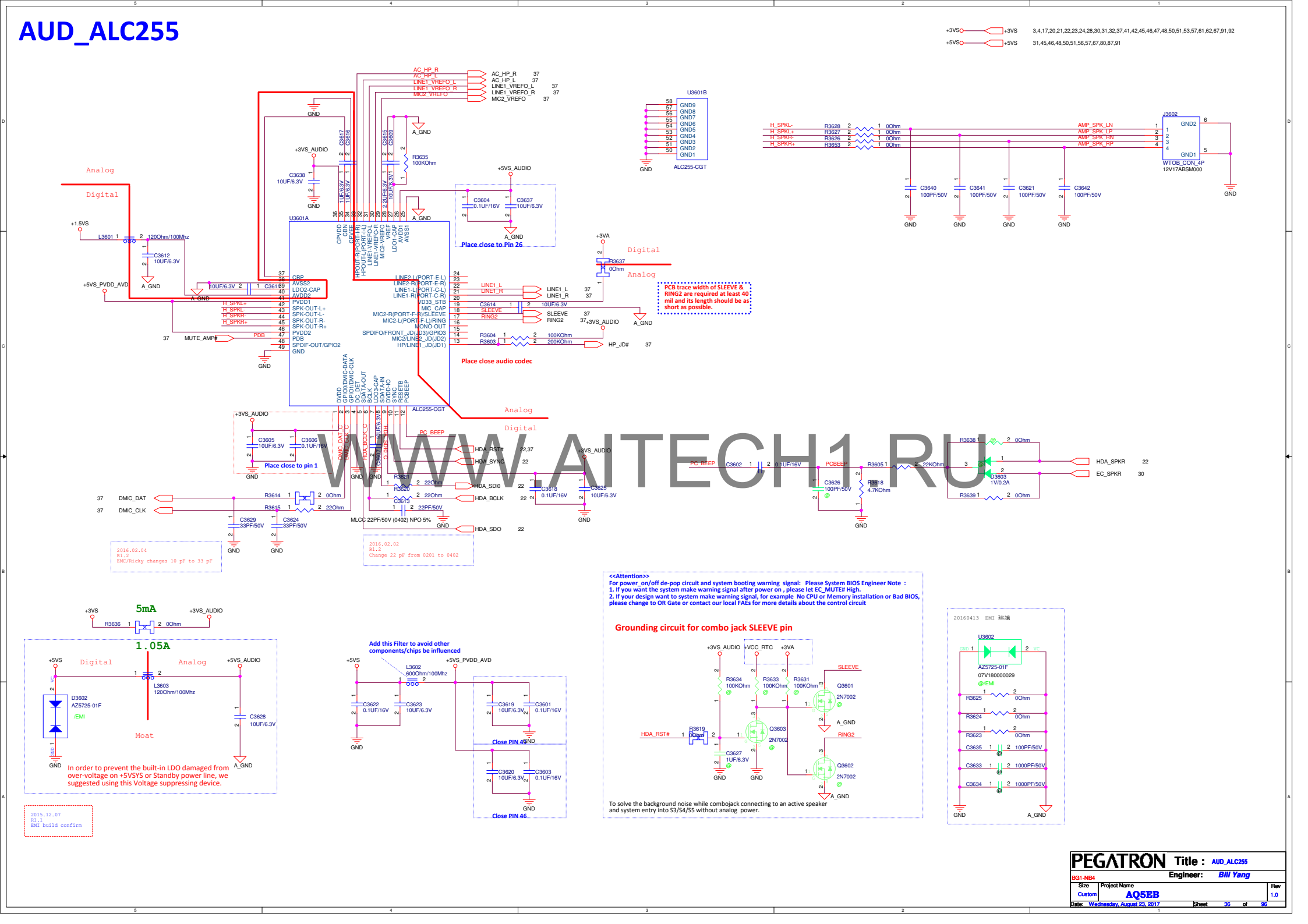
<Title>

Engineer:

| Size | Project Name | Rev |
|---|---|---|
| C | AQ5EB | 1.1 |

Date: Wednesday, August 23, 2017 Sheet 35 of 108

# AUD_ALC255

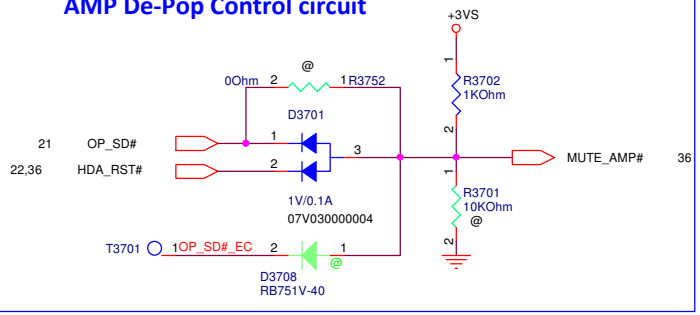


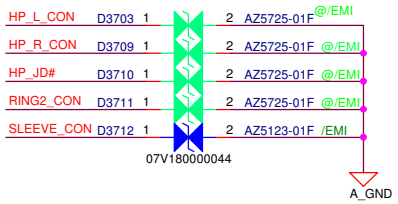


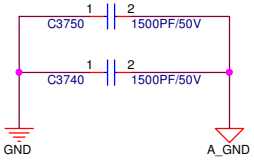

| | | | |
|---|---|---|---|
| PEGATRON | Title : AUD_ALC255 | | |
| BG1-NB4 | Engineer: Bill Yang | | |
| Size: Custom | Project Name: AQ5EB | | Rev: 1.0 |
| Date: Wednesday, August 23, 2017 | Sheet 36 of 96 | | |

+3VS +3VS 3,4,17,20,21,22,23,24,28,30,31,32,36,41,42,45,46,47,48,50,51,53,57,61,62,67,91,92

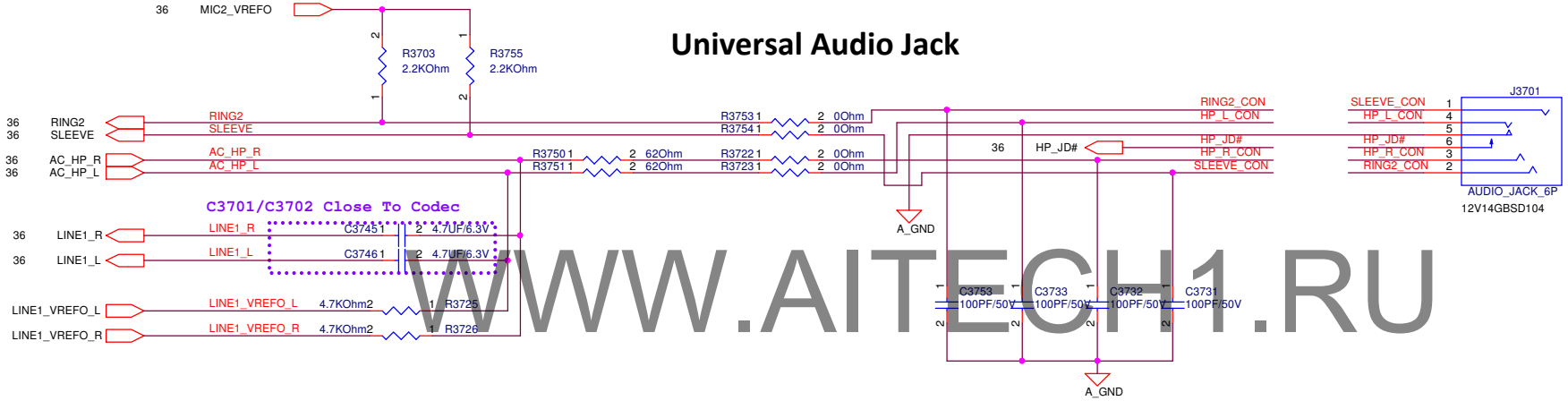
## AMP De-Pop Control circuit



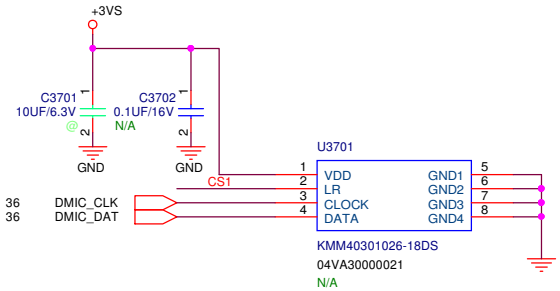




## Universal Audio Jack

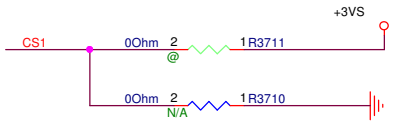


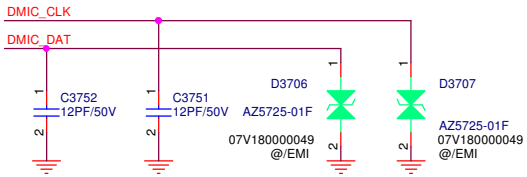



## DMIC




| Single MIC | Left Channel | Right Channel |
|---|---|---|
| CS Pin | Pull Down | Pull Up |




<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : COMBO_JACK
Engineer: Bill Yang
BG1/HW3
Size: Custom
Project Name: AQ5EB
Rev: 1.0
Date: Wednesday, August 23, 2017
Sheet 37 of 108

<Variant Name>

PEGATRON Title :

PEGATRON PROPRIETARY AND CONFIDENTIAL

<Title>

Engineer:

| Size | Project Name | Rev |
|---|---|---|
| C | AQ5EB | 1.1 |

Date: Wednesday, August 23, 2017 Sheet 38 of 108

<Variant Name>

PEGATRON Title :

PEGATRON PROPRIETARY AND CONFIDENTIAL

<Title>

Engineer:

| Size | Project Name | Rev |
|---|---|---|
| C | AQ5EB | 1.1 |

Date: Wednesday, August 23, 2017 Sheet 39 of 108

| | | |
|---|---|---|
| Title | <Title> | |
| Size A | Document Number <Doc> | Rev <RevCode> |
| Date: Wednesday, August 23, 2017 | Sheet 40 of 108 | |

In case of 5V power source for VCON_IN is is equivalent grounded when OFF.
Q4101 is needed to isolate VCON_IN and 5V power source

| | VBUS_DSCHG | SRC_PS_EN | SRC_PS_FLT | SNK_PS_EN | SNK_PS_ACK |
|---|---|---|---|---|---|
| 5440 | GPIO9/ MGPIO2 | GPIO10 | MGPIO8 | GPIO7/ MGPIO3 | GPIO8/ MGPIO1 |

Realtek suggest
C_VMON R41771 @ 2 0Ohm +3V

Realtek suggest
RTS5440 FW was programmed in test mode
+LDO_3V3_CCL R41291 @ 2 0Ohm +3V
VBUS_DSCHG_CTRL T4107 T4108
PD_VBUS_SRC_EN
R4111 4.7KOhm @
R4110 4.7KOhm @
R4112 4.7KOhm @
R4109 4.7KOhm @
R4128 0Ohm @
R10_20170613
Vendor Review
R4111 Reserve (un-mount)

+3V +3V 25,31,44,57,67,82,91
+5VSUS +5VSUS 42,52,56,67,81

+5VSUS
R41171 @ 2 0Ohm +5VCON_IN
Q4101 PJA3411
R4178 47KOhm vx_r0402_small 1%
2N7002 Q4102
MGPIO_DB
R4179 47KOhm vx_r0402_small 1%
R41021 @ 2 0Ohm +5VSUS_CCL
D41051 RB520S-30_G_TE61 If>150mA /Dead Battery
C4124 10UF/25V

42 PD_VBUS_SRC_FLT
42 PD_VBUS_SNK_ACK
42 PD_VBUS_SNK_EN
42 VBUS_DSCHG_CTRL
42 PD_VBUS_SRC_EN
T4104 T4103
PD_VBUS_SRC_FLT

U4101A
10Gbps 3:2 MUX
Low Speed MUX
BC1.2 Switch
Realtek RTS5440
RTS5440 0650-0091000

USB3_RE_RXN SSRX_1P/2N
USB3_RE_RXP SSRX_1N/2P
USB3_RE_TXN SSTX_1P/2N
USB3_RE_TXP SSTX_1N/2P
DDI2_S1_TXN0 C4105 0.1UF/6.3V DDI2_S1_TXN0_C DP0_1P/2N
DDI2_S1_TXP0 C4107 0.1UF/6.3V DDI2_S1_TXP0_C DP0_1N/2P
DDI2_S1_TXN1 C4106 0.1UF/6.3V DDI2_S1_TXN1_C DP1_1P/2N
DDI2_S1_TXP1 C4103 0.1UF/6.3V DDI2_S1_TXP1_C DP1_1N/2P
DDI2_S1_TXN2 C4108 0.1UF/6.3V DDI2_S1_TXN2_C DP2_1P/2N
DDI2_S1_TXP2 C4104 0.1UF/6.3V DDI2_S1_TXP2_C DP2_1N/2P
DDI2_S1_TXN3 C4110 0.1UF/6.3V DDI2_S1_TXN3_C DP3_1P/2N
DDI2_S1_TXP3 C4109 0.1UF/6.3V DDI2_S1_TXP3_C DP3_1N/2P
DPC_S1_AUXP C4113 0.1UF/6.3V DPC_S1_AUXP_C AUX_P/MGPIO4
DPC_S1_AUXN C4114 0.1UF/6.3V DPC_S1_AUXN_C AUX_N/MGPIO5
DPC_S1_HPD HPD
MGPIO_DB MGPIO3 T9305 H_DP/MGPIO2 H_DM/MGPIO3
SM_INT# R41801 2 0Ohm
SMB1_DAT_CFG R41361 2 0Ohm
SMB1_CLK_CFG R41371 2 0Ohm
SM_INT#_CCL SMB1_DAT_CCL SMB1_CLK_CCL
SMB0_DAT SMB0_CLK R41041 @ 2 0Ohm R41011 @ 2 0Ohm
SM_INT/GPIO4 SM_SDA/GPIO6 SM_SCL/GPIO5
R41052 1 6.2KOhm 1% REXT

DB_CFG R41081 @/Dead Battery 2 0Ohm
CC1 UTC_A5_CC1 C4122 2 220PF/50V
CC2 UTC_B5_CC2 C4123 2 220PF/50V
C_TX2_1P/2N UTC_B3_SSTXn2
C_TX2_1N/2P UTC_B2_SSTXp2
C_RX2_1P/2N UTC_A10_SSRXn2
C_RX2_1N/2P UTC_A11_SSRXp2
C_TX1_1P/2N UTC_A3_SSTXn1
C_TX1_1N/2P UTC_A2_SSTXp1
C_RX1_1P/2N UTC_B10_SSRXn1
C_RX1_1N/2P UTC_B11_SSRXp1
SBU1/MGPIO6 UTC_A8_SBU1_AUX
SBU2/MGPIO7 UTC_B8_SBU2_AUX
C_DP/BB_DP USB_PP4_FW R41072 1 0Ohm T4105
C_DM/BB_DM USB_PM4_FW R41062 1 0Ohm T4106

UTC_A5_CC1 UTC_B5_CC2
D4101 AZ4024-01F
D4102 AZ4024-01F
Reserved ESD Components

+LDO_3V3_CCL R41231 @ 2 0Ohm +5VSUS_CCL

NOTE:
1.If the 5V_IN power supply voltage is fixed 5V or variable from 3.3V to 5V. Remove the 0ohm resistor.
2.If the 5V_IN power supply voltage is fixed 3.3V, stuff the 0ohm resistor

C4115 4.7UF/10V C4116 0.1UF/16V C4117 10UF/25V
+LDO_3V3_CCL +5VSUS_CCL +5VCON_IN

R10_20170613
Vendor Review
Mount R4115

+LDO_3V3_CCL +AC_BAT_SYS VBUS_USB_TYPE_C
R4119 54.9KOHM @ 10V220000202
R4115 590KOhm 1%
R4113 200KOhm 1%
C_LOC_PWR C_VMON
R4118 10KOhm 1%
R4114 10KOhm 1%
R4116 10KOhm 1%
GND

R10_20170613
Vendor Review
SMBus PU 4.7K ohm to +LDO_3V3_CCL

SMB1_DAT_CCL R4150 2 1 4.7KOhm +LDO_3V3_CCL
SMB1_CLK_CCL R4151 2 1 4.7KOhm
SM_INT#_CCL R4103 2 1 4.7KOhm

+LDO_3V3_CCL
DPC_S1_AUXN_C R4122 2 1 100KOhm
DPC_S1_AUXP_C R4120 2 1 100KOhm
DPC_S1_HPD R4121 2 1 100KOhm
GND

+3VS
DPC_S1_AUXN R4126 2 N/A 1 100KOhm
DPC_S1_AUXP R4127 2 N/A 1 100KOhm
GND

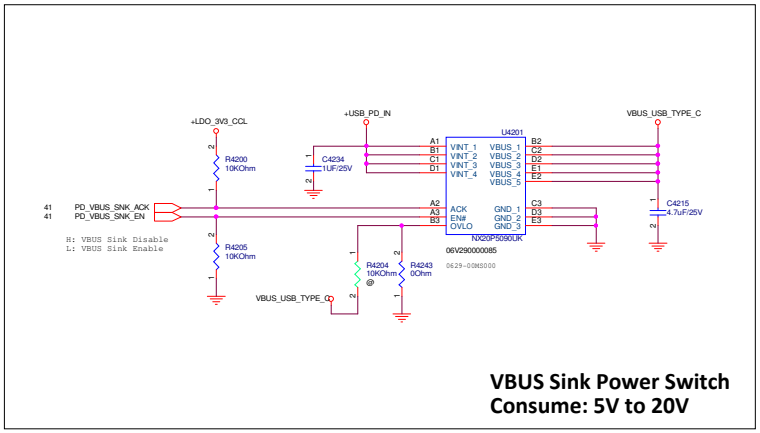
U4101B
GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8
RTS5440 0650-0091000
GND

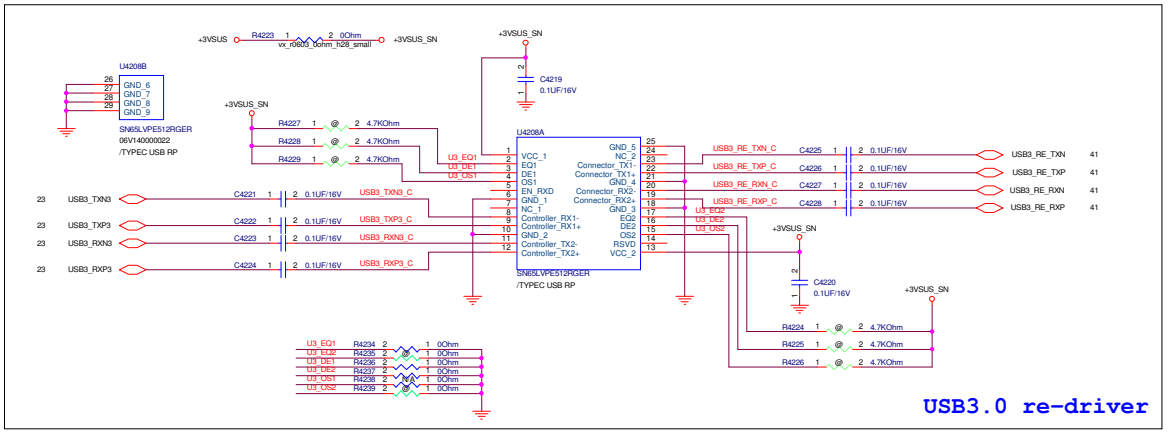
| RTS5440---> | Slave Addr | R4119 | R4118 |
|---|---|---|---|
| | 0XAC | NC | 10K |
| | 0XAE | 54.9K | 12.1K |
| | 0XB0 | 27.4K | 15.8K |
| | 0XB2 | 18.2K | 22.1K |

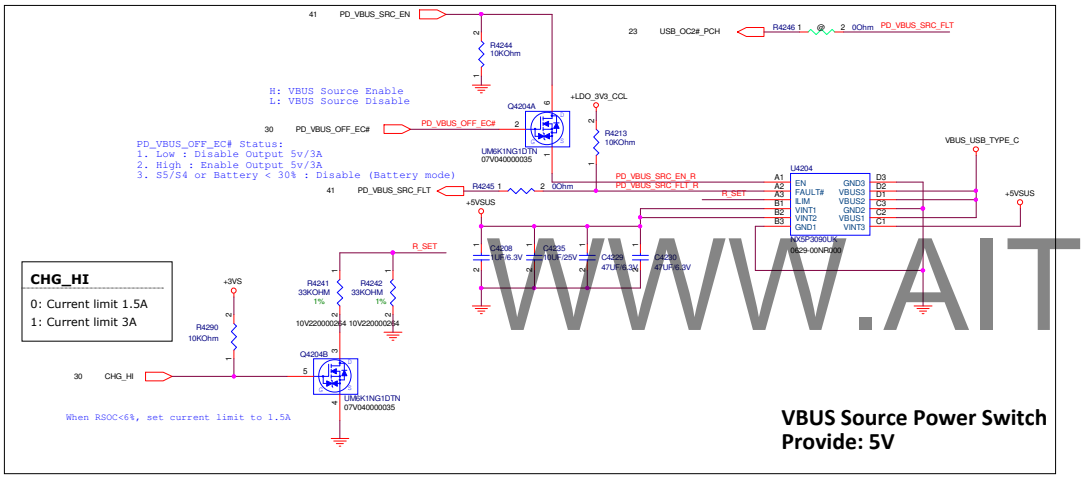
R4114, R4115, R4118, R4119 must be precision resistor of 1%.

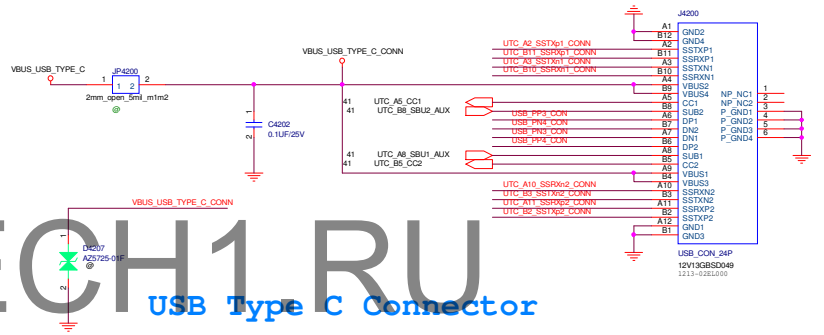
<Variant Name>

PEGATRON Title :POWER_FLOWCHART
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Bill Yang
Size Custom | Project Name AQ5EB | Rev 1.0
Date: Wednesday, August 23, 2017 Sheet 41 of 97

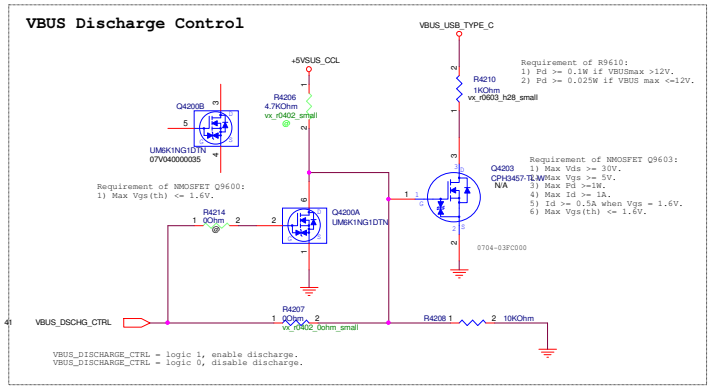


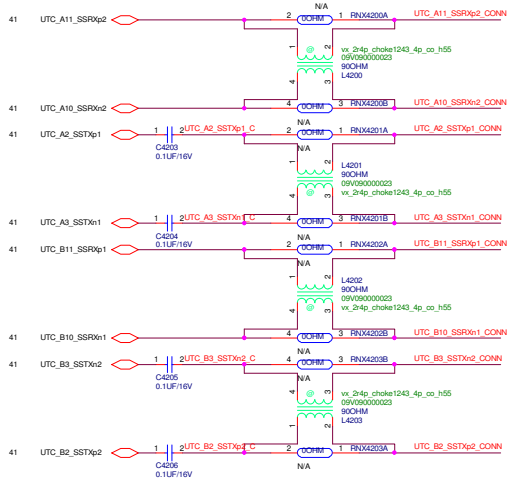



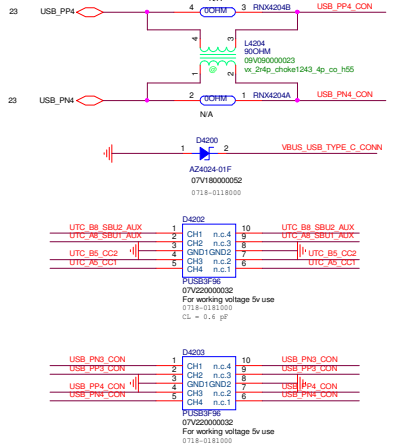



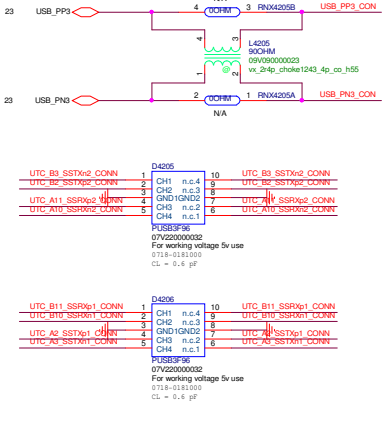



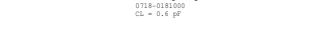

| A1 | A2 | A3 | A4 | A5 | A6 | A7 | A8 | A9 | A10 | A11 | A12 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| GND | TX1+ | TX1- | Vbus | CC1 | D+ | D- | SBU1 | Vbus | RX2- | RX2+ | GND |
| GND | RX1+ | RX1- | Vbus | SBU2 | D- | D+ | CC2 | Vbus | TX2- | TX2+ | GND |
| B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 |











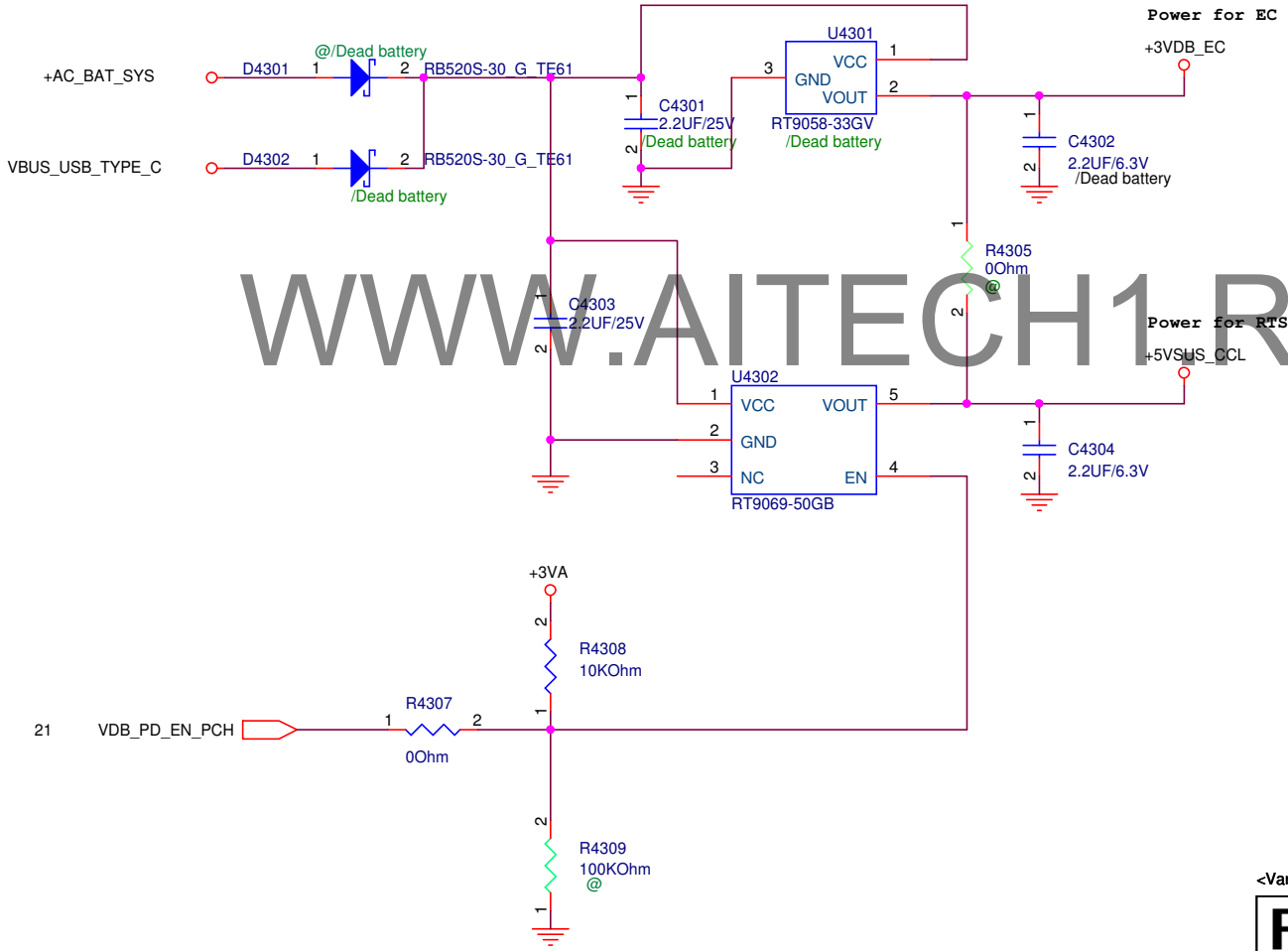

PEGATRON Title: USB Type-C Receptacle
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Bill Yang
Size: Custom | Project Name: AQ5EB | Rev: 1.0
Date: Wednesday, August 23, 2017 | Sheet 42 of 108

# Hardware Solution For Dead Battery

For notebook applications, if the battery charger needs higher voltage than
5V to operate correctly, execute the steps below in the order they are listed:

| | | | |
|---|---|---|---|
| VBUS_USB_TYPE_C | VBUS_USB_TYPE_C | 41,42 |
| +AC_BAT_SYS | +AC_BAT_SYS | 41,45,80,81,82,83,85,87,88 |
| +3VDB_EC | +3VDB_EC | 30 |
| +5VSUS_CCL | +5VSUS_CCL | 41,42 |

Requirement of U1:
1) Vin range: 4V~30V.
2) Vout: EC's operating voltage + Vf of D1
3) Output current >= EC's operating current.






<Variant Name>

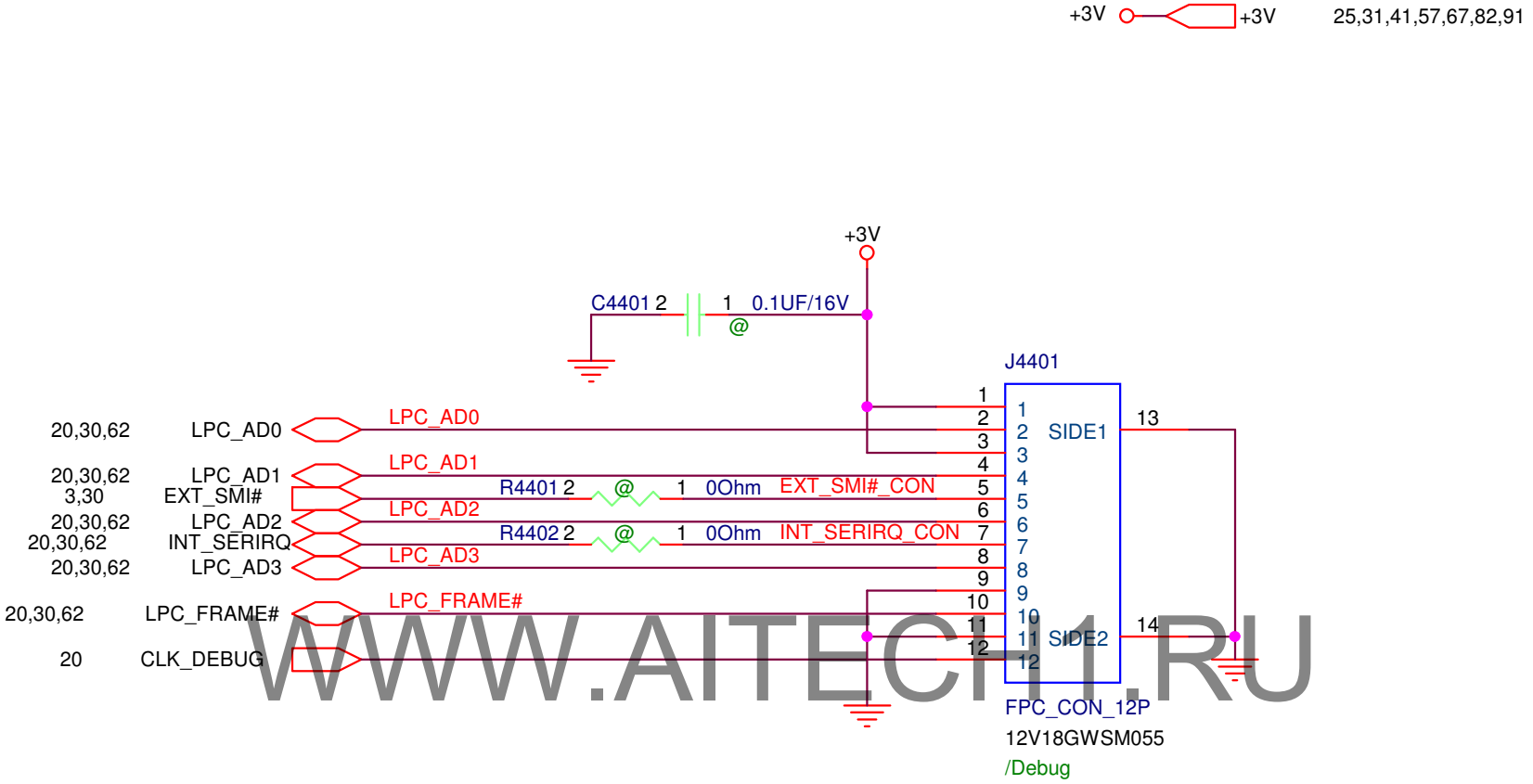
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : Dead Battery

Engineer: Bill Yang

| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 1.0 |

Date: Wednesday, August 23, 2017 Sheet 43 of 97






<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : BUG_Debug

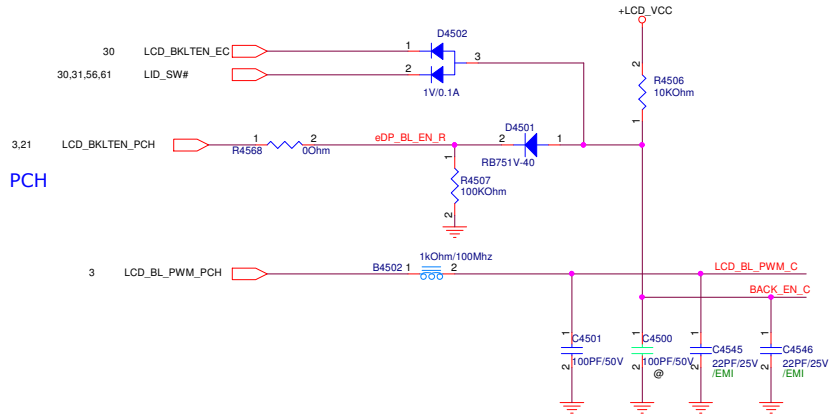
Engineer: Bill Yang

BG1/HW3

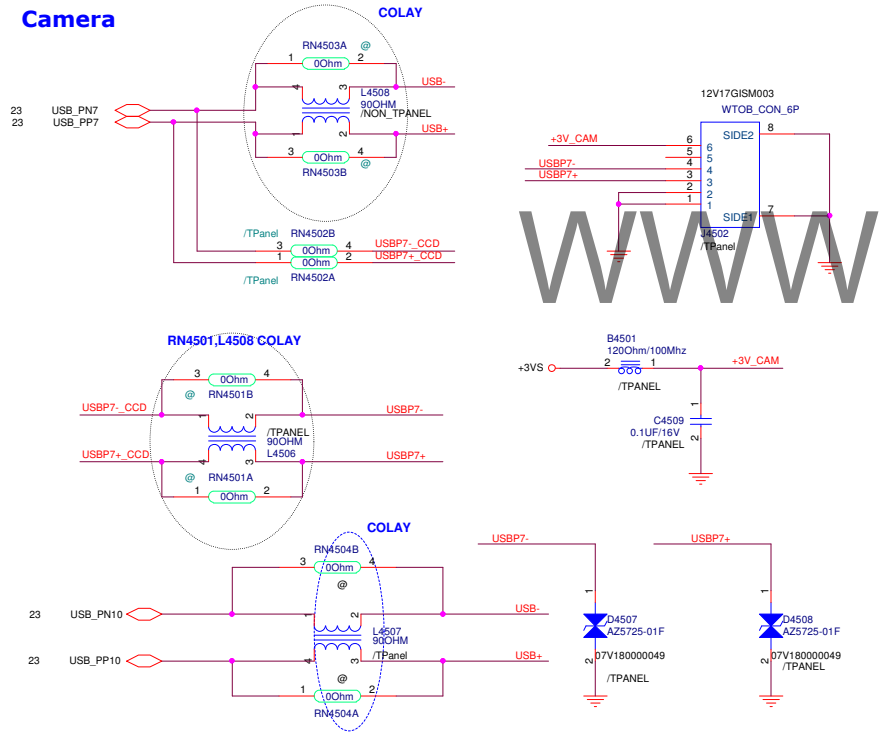
| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 1.0 |

Date: Wednesday, August 23, 2017 Sheet 44 of 108

## Controller circuit



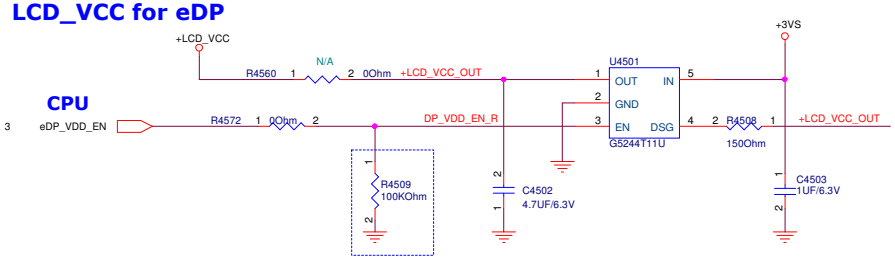

## Camera



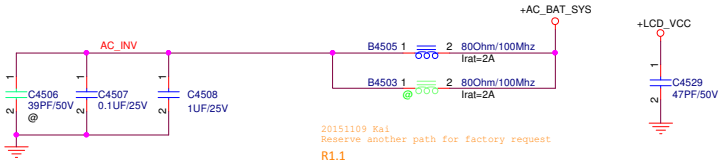

## eDP HPD



## LCD_VCC for eDP

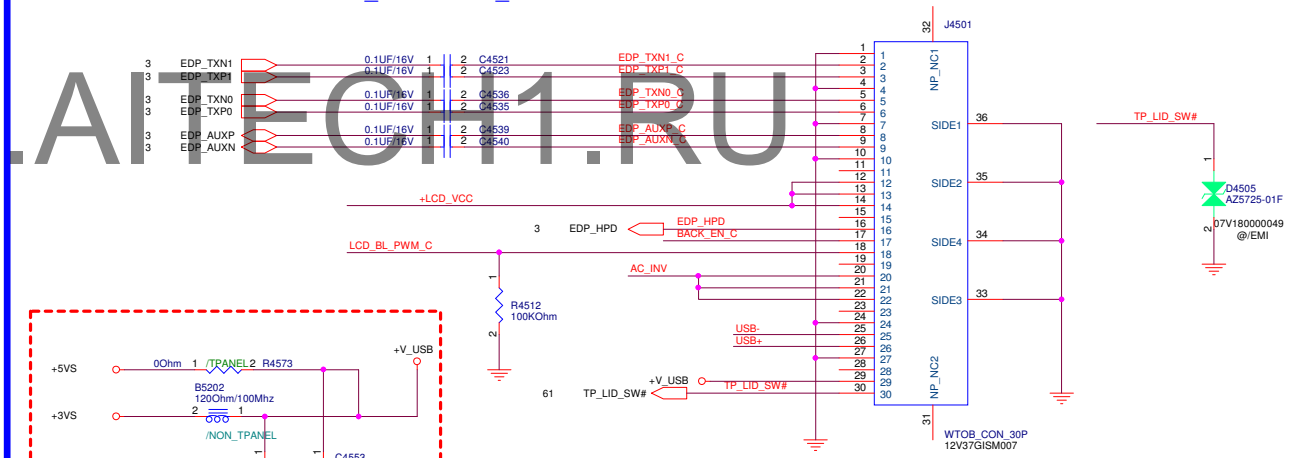



## Check PCH/FCH or CPU PD




## eDP Connector

NOTE:
Entire trace of Panel_VCC & LCD_VCC should be wider than 80-mil






PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : LVDS Out

BG1\HW3

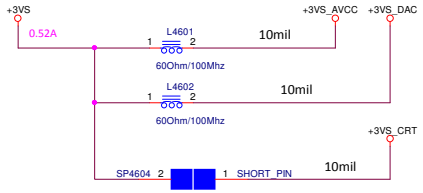
Engineer: Bill Yang

| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 1.0 |

Date: Wednesday, August 23, 2017 Sheet 45 of 108

# DP2VGA Realtek RTD2166

## Power




## Rom / Flash Mode :

| | | POL1 (Pin10) | |
|---|---|---|---|
| | | **0** | 1 |
| POL2 (Pin9) | 0 | No Use | No Use |
| | **1** | **(V) Rom mode** | Ext Flash mode |

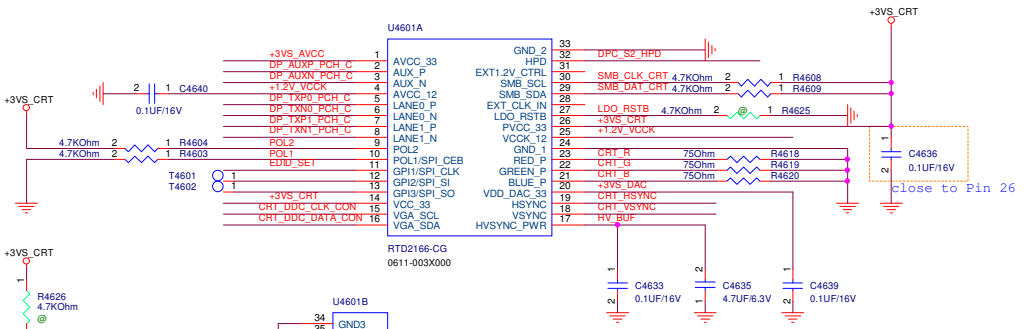
## Embedded EDID setting :

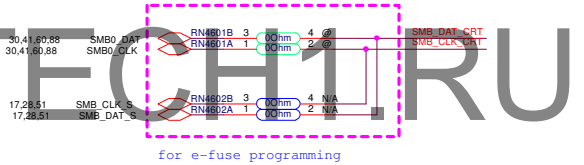
| EDID_SET (Pin11) | Mode |
|---|---|
| **0 or NC** | **(V) Disable RTD2166 Embedded EDID** |
| 1 | Enable RTD2166 Embedded EDID |

## LDO Mode :

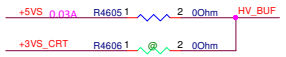
| LDO_RSTB (Pin27) | Mode |
|---|---|
| **1 or NC** | **(V) embedded LDO Mode** |
| 0 | External 1.2V Mode |

**1: Pull High  0: Pull Down**



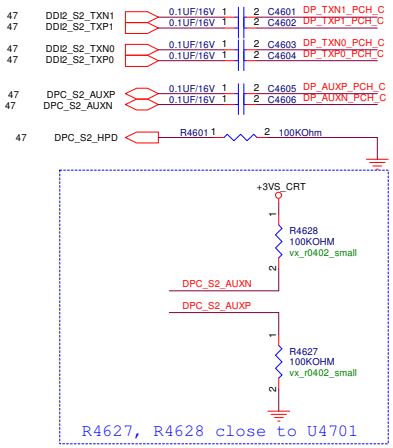



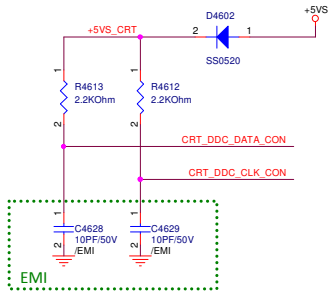

CRT_HV Sync Voltage setting :
R4605 : 5V
R4606 : 3.3V



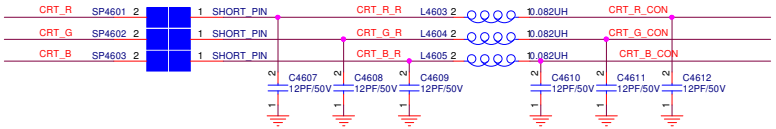
## CPU Interface

DP main link total length < 8 inch
VIA < 2

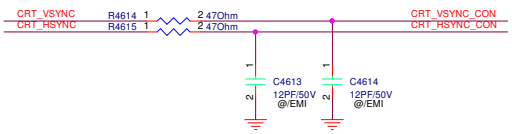


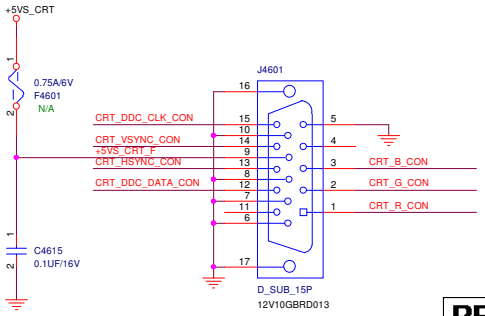

Max mismatch between RGB signal < 200 mil,
total trace length < 6 inch




CRT_HV Sync total trace length < 6 inch

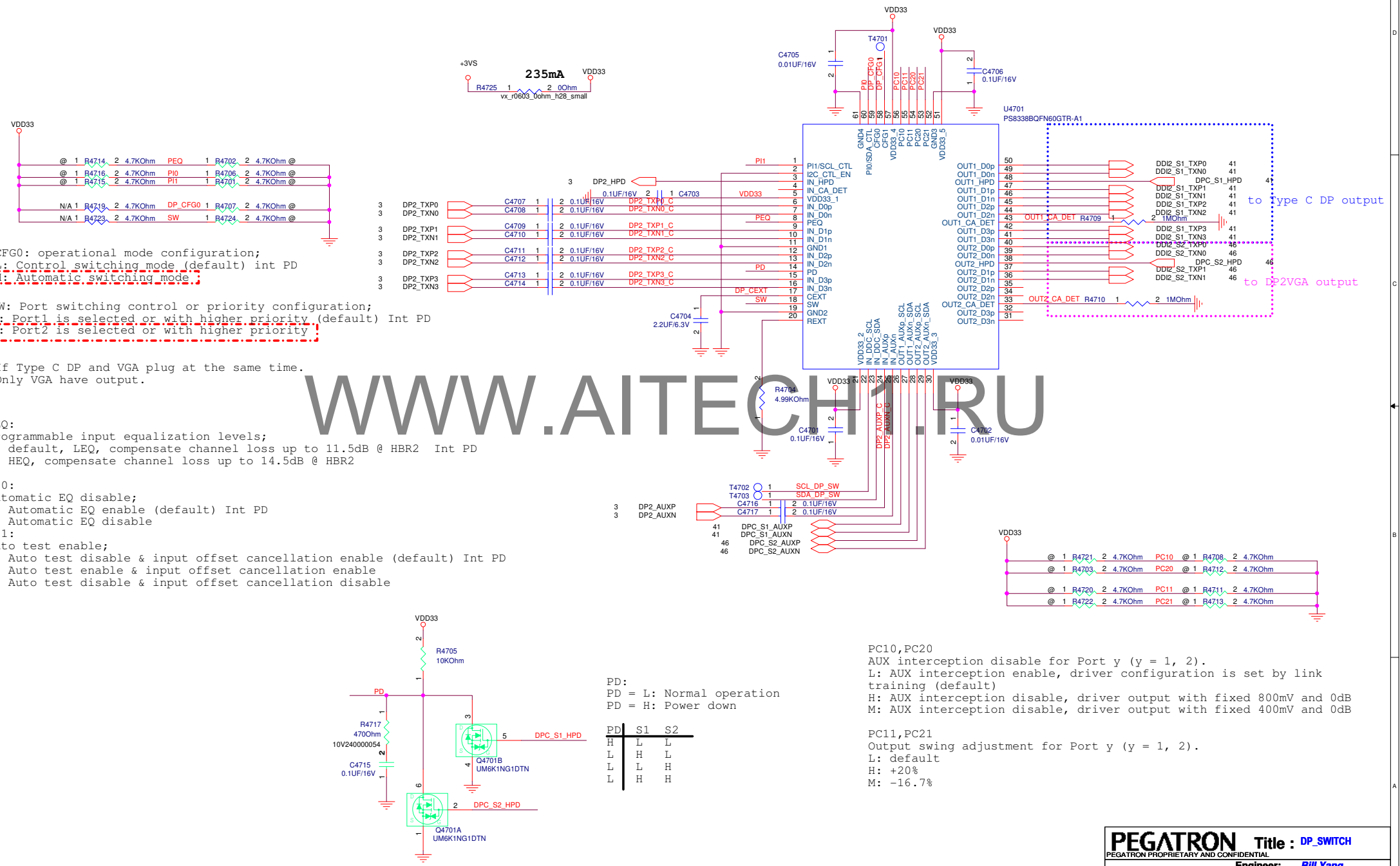



## D-SUB Connector






PEGATRON Title : CRT RTD2166
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Bill Yang
<OrgName>
Size: Custom | Project Name: AQ5EB | Rev: 1.0
Date: Wednesday, August 23, 2017 | Sheet 46 of 104




CFG0: operational mode configuration;
L: Control switching mode (default) int PD
H: Automatic switching mode

SW: Port switching control or priority configuration;
L: Port1 is selected or with higher priority (default) Int PD
H: Port2 is selected or with higher priority

If Type C DP and VGA plug at the same time.
Only VGA have output.

PEQ:
Programmable input equalization levels;
L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2 Int PD
H: HEQ, compensate channel loss up to 14.5dB @ HBR2

PI0:
Automatic EQ disable;
L: Automatic EQ enable (default) Int PD
H: Automatic EQ disable
PI1:
Auto test enable;
L: Auto test disable & input offset cancellation enable (default) Int PD
H: Auto test enable & input offset cancellation enable
M: Auto test disable & input offset cancellation disable

PD:
PD = L: Normal operation
PD = H: Power down

| PD | S1 | S2 |
|---|---|---|
| H | L | L |
| L | H | L |
| L | L | H |
| L | H | H |

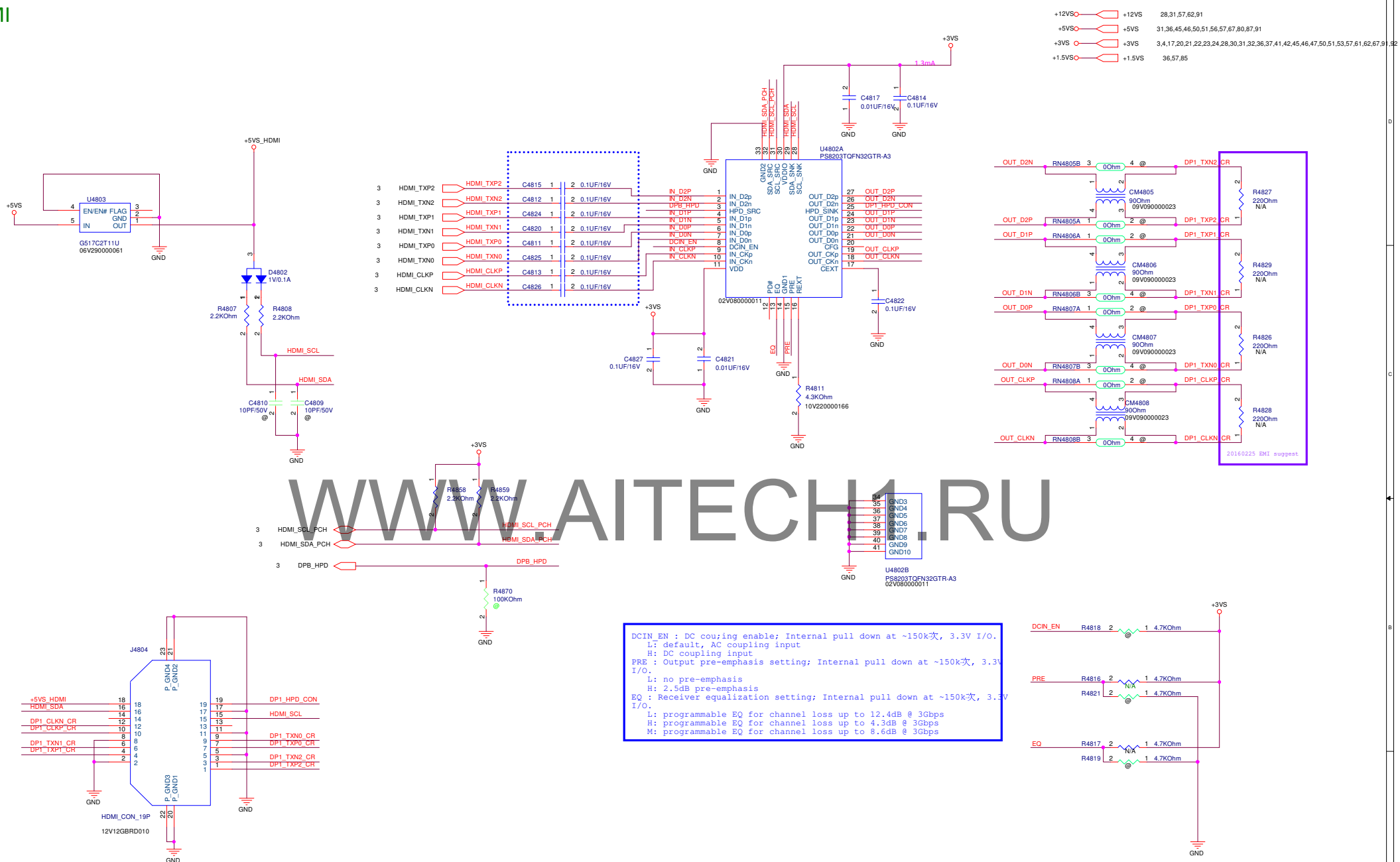
PC10,PC20
AUX interception disable for Port y (y = 1, 2).
L: AUX interception enable, driver configuration is set by link training (default)
H: AUX interception disable, driver output with fixed 800mV and 0dB
M: AUX interception disable, driver output with fixed 400mV and 0dB

PC11,PC21
Output swing adjustment for Port y (y = 1, 2).
L: default
H: +20%
M: -16.7%



PEGATRON Title : DP_SWITCH
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Bill Yang
BG1/HW3
Size Custom | Project Name AQ5EB | Rev 1.0
Date: Wednesday, August 23, 2017 Sheet 47 of 108

# HDMI






<Variant Name>

PEGATRON Title : HDMI-4K2K

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3 Engineer: Bill Yang

| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 1.0 |

Date: Wednesday, August 23, 2017 Sheet 48 of 108

<Variant Name>

PEGATRON Title :



<Title>

Engineer:

| Size | Project Name | Rev |
|---|---|---|
| C | AQ5EB | 1.1 |

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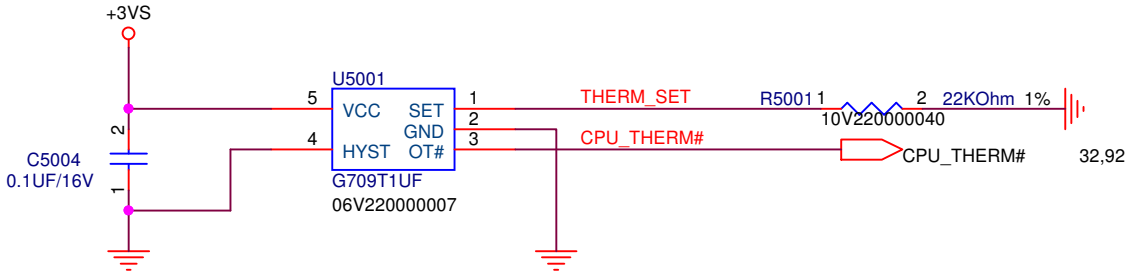
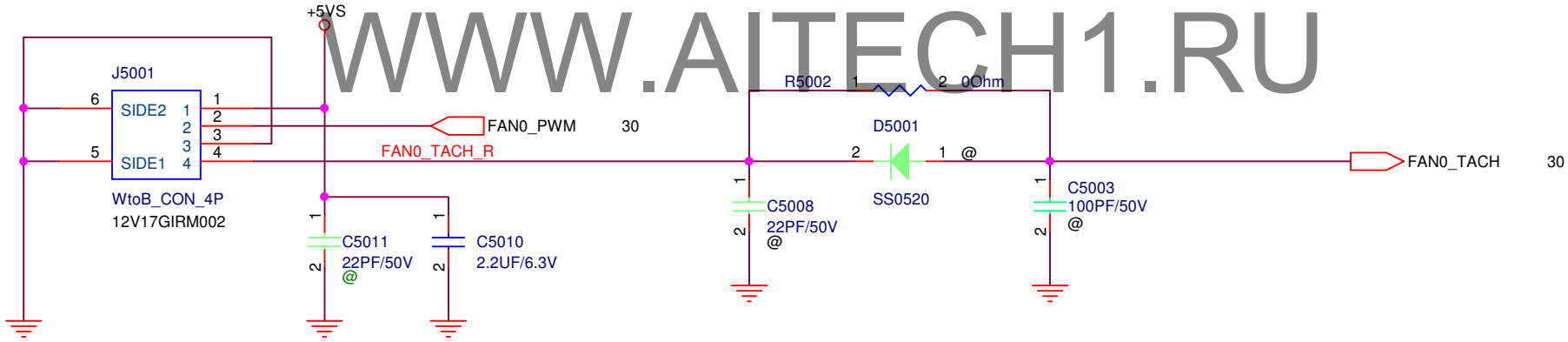
+3VS +3VS 3,4,17,20,21,22,23,24,28,30,31,32,36,37,41,42,45,46,47,48,51,53,57,61,62,67,91,92

+5VS +5VS 31,36,45,46,48,51,56,57,67,80,87,91






PEGATRON PROPRIETARY AND CONFIDENTIAL

Title THERMAL/ FAN

Engineer: Bill Yang

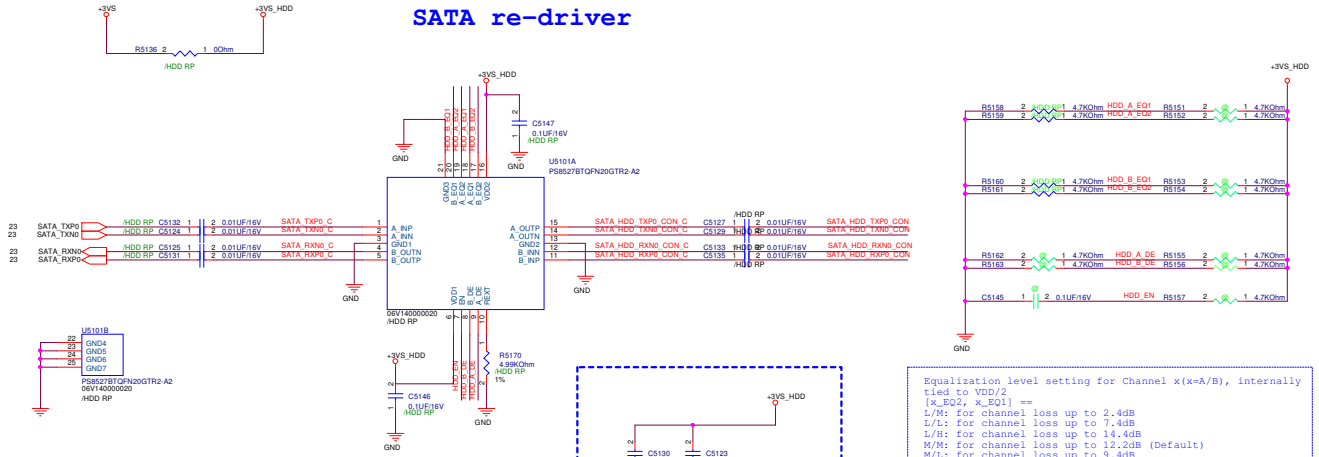
BG1/HW3

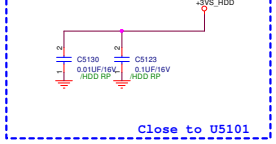
Size Custom | Project Name AQ5EB | Rev 1.0

Date: Wednesday, August 23, 2017 | Sheet 50 of 108

# HDD

## SATA re-driver



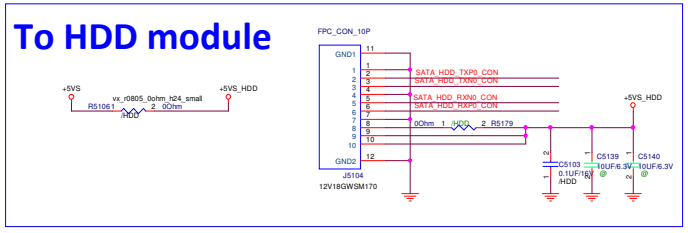




Equalization level setting for Channel x(x=A/B), internally tied to VDD/2
[x_EQ2, x_EQ1] ==
L/M: for channel loss up to 2.4dB
L/L: for channel loss up to 7.4dB
L/H: for channel loss up to 14.4dB
M/M: for channel loss up to 12.2dB (Default)
M/L: for channel loss up to 9.4dB
M/H: for channel loss up to 13.3dB
H/M: for channel loss up to 6.2dB
H/L: for channel loss up to 11.2dB
H/H: for channel loss up to 5dB

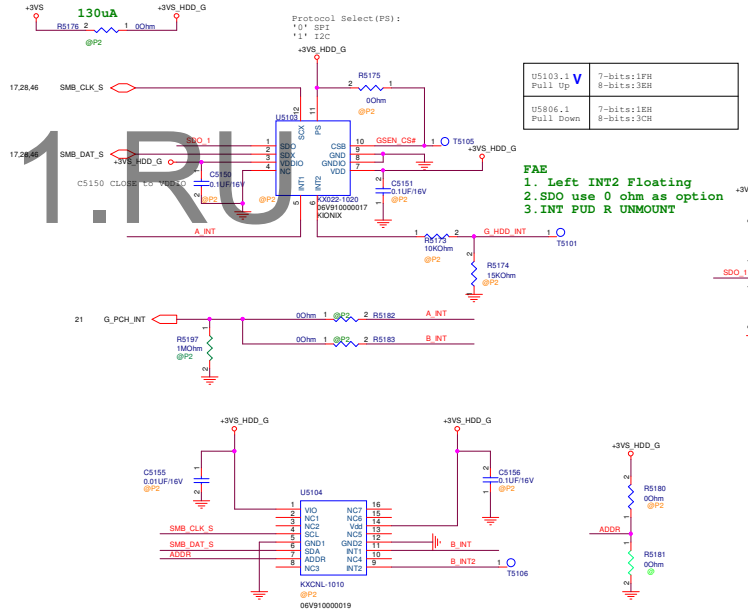
De-emphasis level setting for Channel x(x=A/B), internally tied to VDD/2
[x_DE] ==
M: -3.5dB (Default)
L: 0dB
H: -6dB

## To HDD module



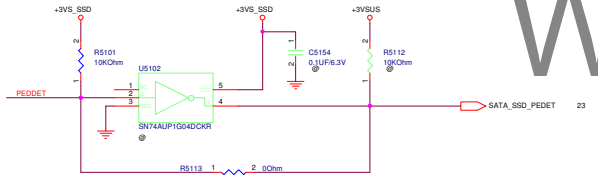

+3VS 3,4,17,20,21,22,23,24,28,30,31,32,36,37,41,42,45,46,47,48,50,53,57,61,62,67,91,92
+5VS 31,36,45,46,48,50,56,57,67,80,87,91
+5VSUS 41,42,52,56,67,81

## HDD G-Sensor

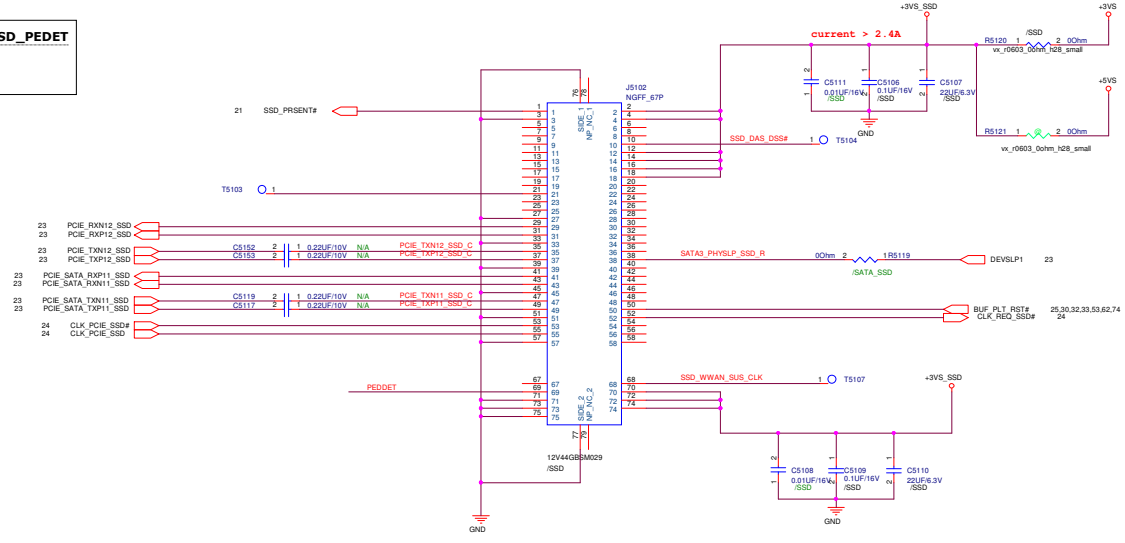



FAE
1. Left INT2 Floating
2.SDO use 0 ohm as option
3.INT PUD R UNMOUNT

## SSD(SATA/PCIE x2) NGFF socket (M-key)




**SATA_SSD_PEDET**
0: SATA
1: PCIE






<variant_name>

PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : SATA HDD/ODD
Engineer: Bill Yang
BG1/HW3
Size: Custom
Project Name: AQ5EB
Rev: 1.0
Date: Wednesday, August 23, 2017
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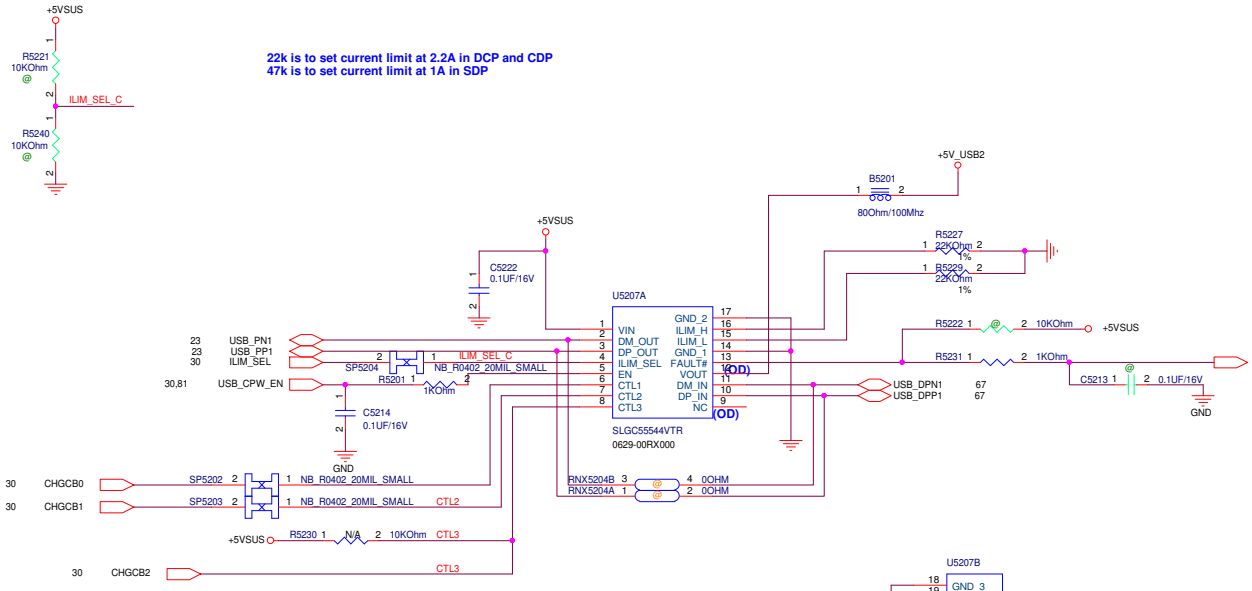
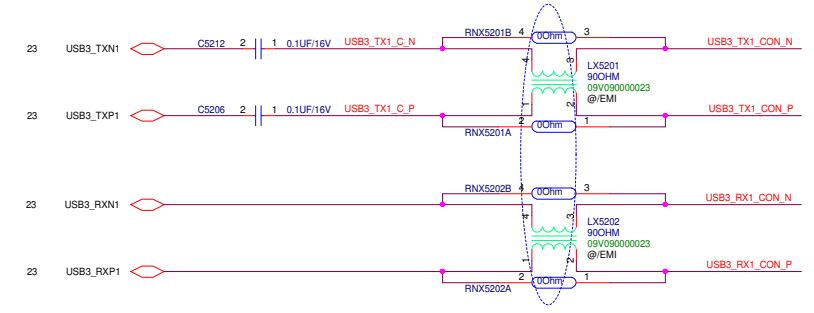
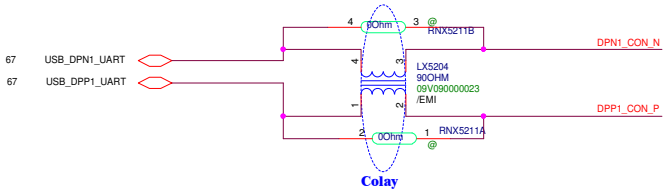
# USB 3.0 ports x 1 with Sleep & Charge Left_Down

## TPS2544 Device True Table

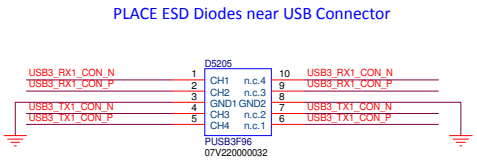


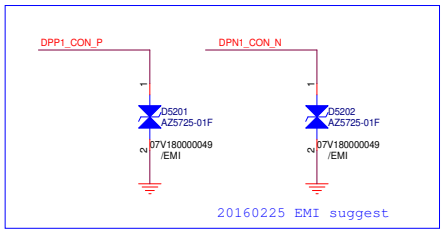



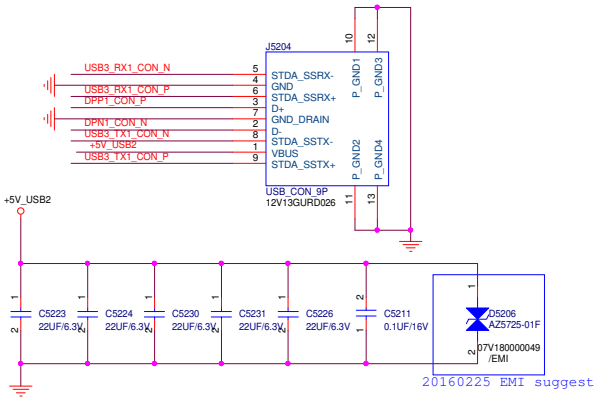






| System Global Power State | TPS2544 Charging Mode | CTL1 | CTL2 | CTL3 | ILIM_SEL | Current Limit Setting |
|---|---|---|---|---|---|---|
| S0 | SDP (Standard Downstream) | 1 | 1 | 0 | 1 or 0 | ILIM_HI / ILIM_LO |
| S0 | SDP, no discharge to / from CDP | 1 | 1 | 1 | 0 | ILIM_LO |
| S0 | CDP, if a BC1.2 primary detection occurs | 1 | 1 | 1 | 1 | ILIM_HI |
| S3/S4/S5 | Auto mode, no mouse wake | 0 | 0 | 1 | 0 | ILIM_HI |
| S3 | Dedicated Charging Port Auto mode, keyboard/mouse wake up | 0 | 1 | 1 | X | ILIM_HI |
| S3 | SDP, keyboard/ mouse wake-up | 0 | 1 | 0 | 1 or 0 | ILIM_HI / ILIM_LO |





PEGATRON Title : USB JACK

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3 Engineer: Bill Yang

| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 1.0 |

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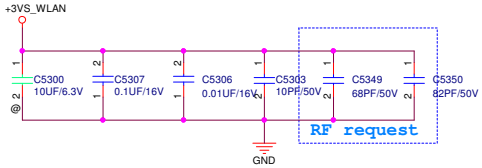
# WLAN/ WiGig / BT

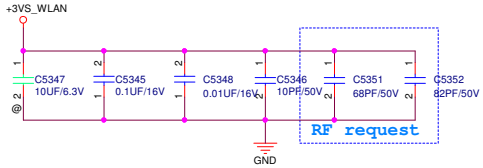
**+3V_WLAN_WP1 bypass capactor:**
Place 0.1UF near pin 2,4

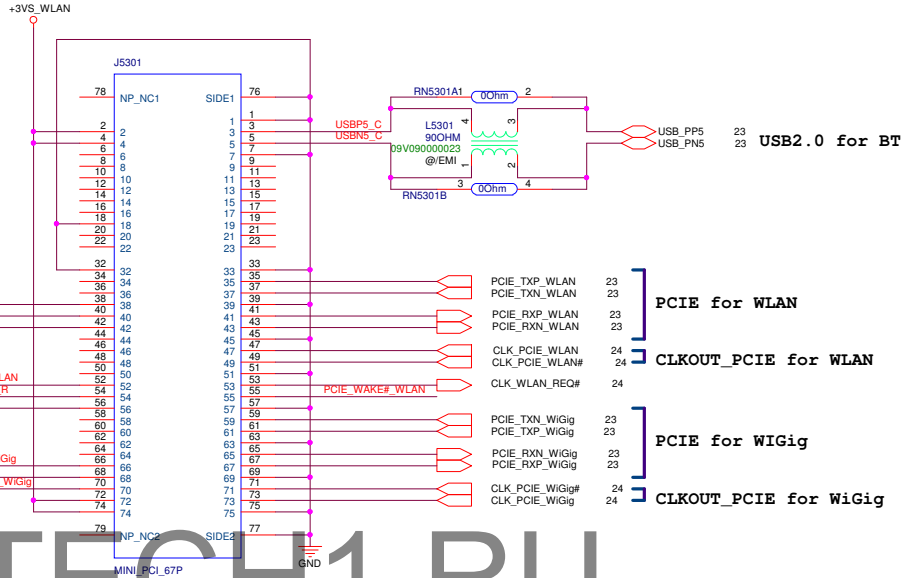
Place 10UF near +3V_WLAN_WP1 source side.

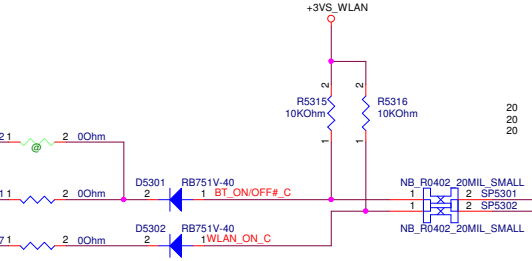
**+3V_WLAN_WP1 bypass capactor:**
Place 0.1UF near pin 72,74.

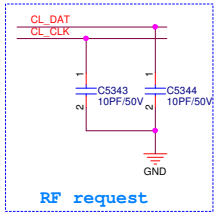
Place 10UF near +3V_WLAN_WP1 source side.



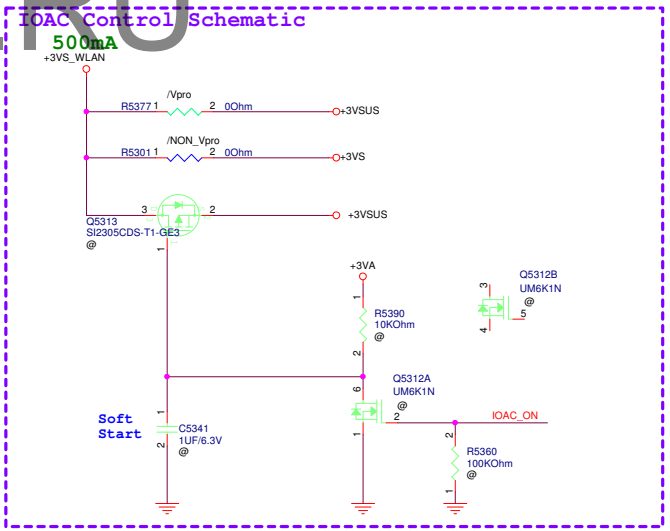



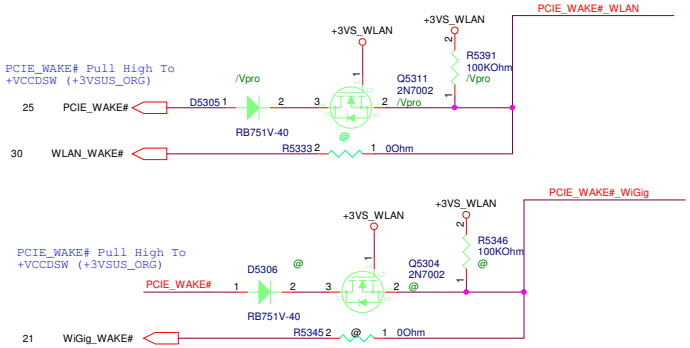



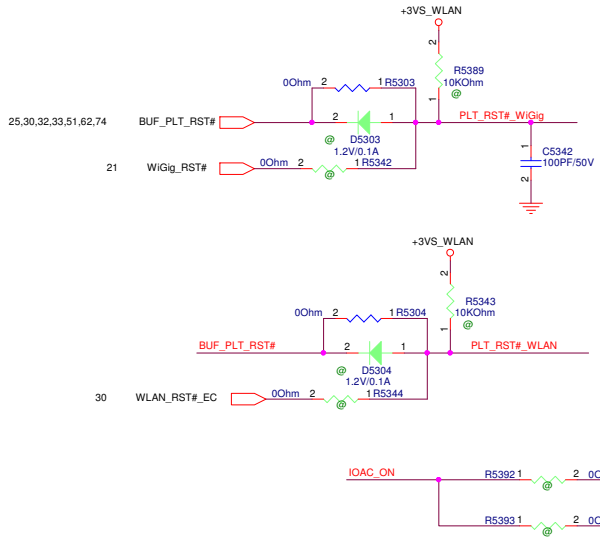













<Variant Name>

PEGATRON Title : WLAN/ WiGig / BT
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1/HW4 Engineer: Bill Yang

| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 1.0 |

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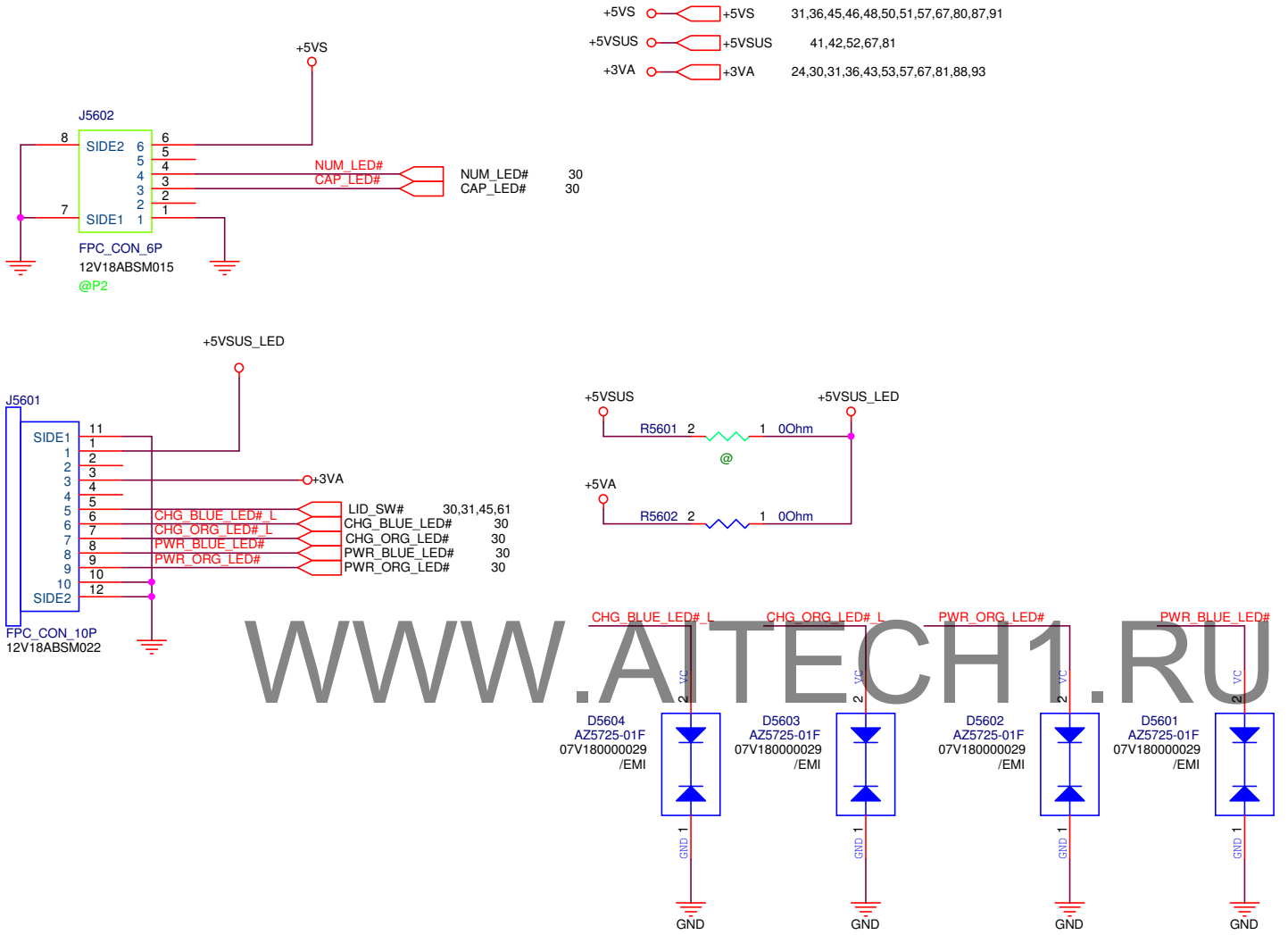
| | | |
|---|---|---|
| Title <Title> | | |
| Size A | Document Number <Doc> | Rev <RevCode> |
| Date: Wednesday, August 23, 2017 | Sheet 54 of 108 | |

| | | |
|---|---|---|
| Title | <Title> | |
| Size: A | Document Number: AQ5EB | Rev: 1.1 |
| Date: Wednesday, August 23, 2017 | Sheet 55 of 108 | |






PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : LED

Engineer: Bill Yang

BG1/HW3

| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 1.0 |

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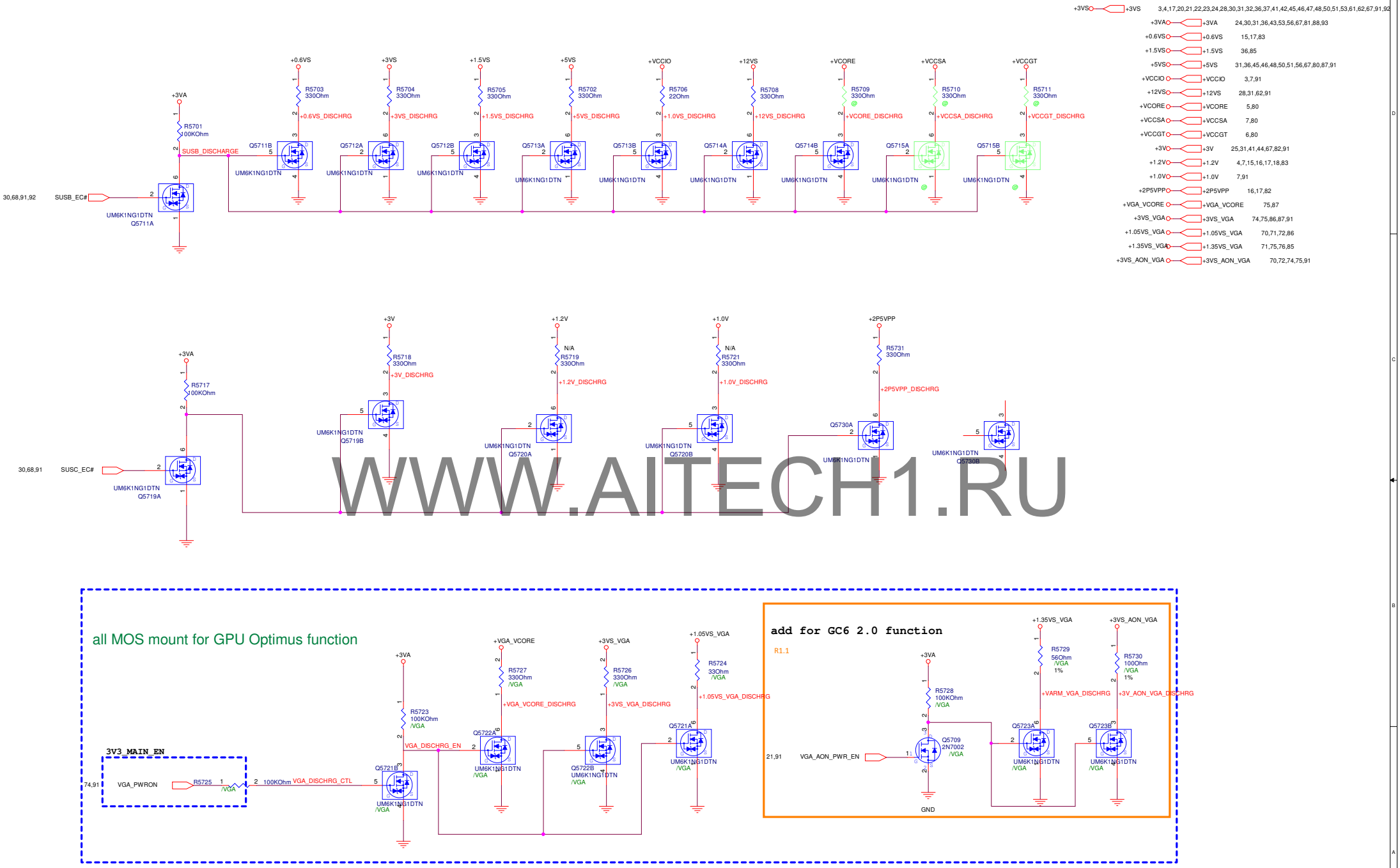




PEGATRON Title : DSG_Discharge

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Bill Yang

| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 1.0 |

Date: Wednesday, August 23, 2017 Sheet 57 of 108

| | | |
|---|---|---|
| Title | <Title> | |
| Size A | Document Number AQ5EB | Rev <RevCode> |
| Date: Wednesday, August 23, 2017 | Sheet 58 of 108 | |

<Variant Name>

PEGATRON Title :

PEGATRON PROPRIETARY AND CONFIDENTIAL

<Title>

Engineer:

| Size | Project Name | Rev |
|---|---|---|
| C | AQ5EB | 1.1 |

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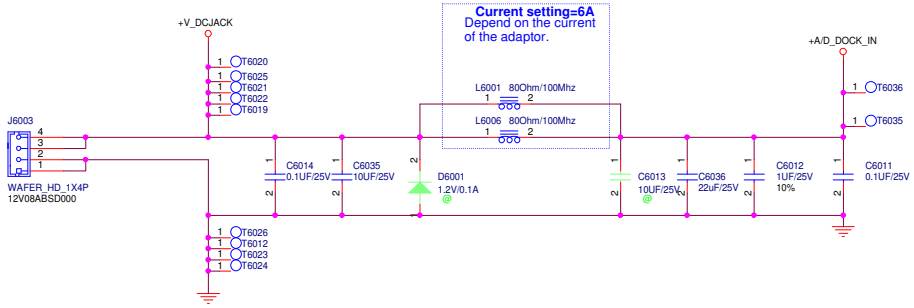
# 60

# DC_BAT_CONN

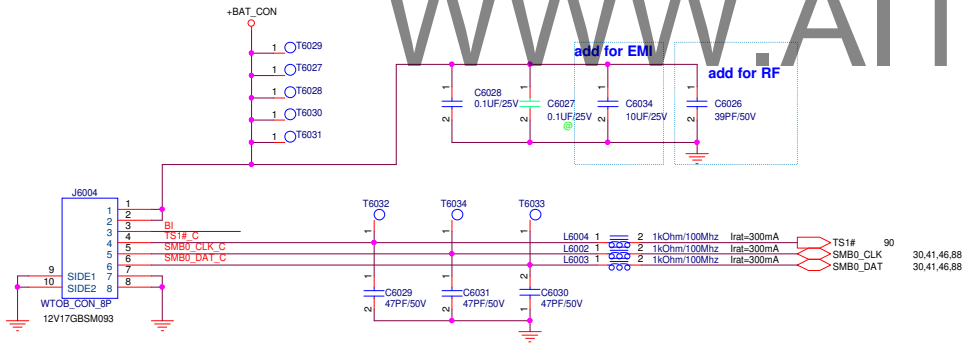
## DC Jack WTB CONN

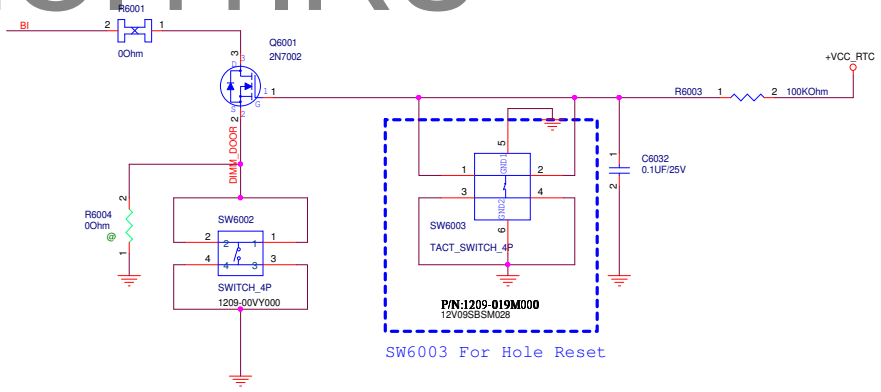


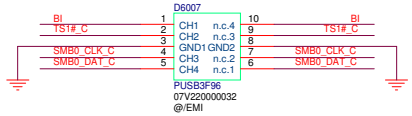

| | | |
|---|---|---|
| +VCC_RTC | +VCC_RTC | 24,25,26,36 |
| +3VA_EC | +3VA_EC | 28,30,32 |
| +3VA | +3VA | 24,30,31,36,43,53,56,57,67,81,88,93 |
| +5VA | +5VA | 31,56,81 |
| +1.0VSUS | +1.0VSUS | 26,82 |
| +1.8VSUS | +1.8VSUS | 9,21,24,26,84 |
| +3VSUS | +3VSUS | 4,24,25,26,28,30,31,33,42,51,53,62,67,68,81,92 |
| +5VSUS | +5VSUS | 41,42,52,56,67,81 |
| +12VSUS | +12VSUS | 81,91 |
| +3V | +3V | 25,31,41,44,57,67,82,91 |
| +12V | +12V | 91 |
| +3VS | +3VS | 3,4,17,20,21,22,23,24,28,30,31,32,36,37,41,42,45,46,47,48,50,51,53,57,61,62,67,91,92 |
| +5VS | +5VS | 31,36,45,46,48,50,51,56,57,67,80,87,91 |
| +12VS | +12VS | 28,31,57,62,91 |
| +AC_BAT_SYS | +AC_BAT_SYS | 41,43,45,80,81,82,83,85,87,88 |
| +A/D_DOCK_IN | +A/D_DOCK_IN | 89 |
| +BAT_CON | +BAT_CON | 88 |
| +VCORE | +VCORE | 5,57,80 |
| +VCCGT | +VCCGT | 6,57,80 |
| +VCCSA | +VCCSA | 7,57,80 |
| +VCCIO | +VCCIO | 3,7,57,91 |
| +RTCBAT | +RTCBAT | 24 |

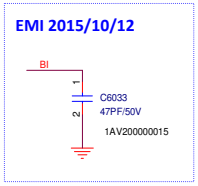
## Battery Connector






PEGATRON Title : DC_BAT_CONN

BG1-HW3 Engineer: Bill Yang

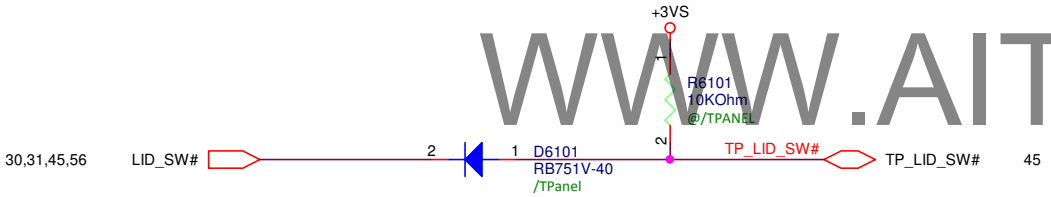
| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 1.0 |

Date: Wednesday, August 23, 2017 Sheet 60 of 108

+5VS +5VS 31,36,45,46,48,50,51,56,57,67,80,87,91

+3VS +3VS 3,4,17,20,21,22,23,24,28,30,31,32,36,37,41,42,45,46,47,48,50,51,53,57,62,67,91,92






<Variant Name>

PEGATRON Title : Touch Panel Conn

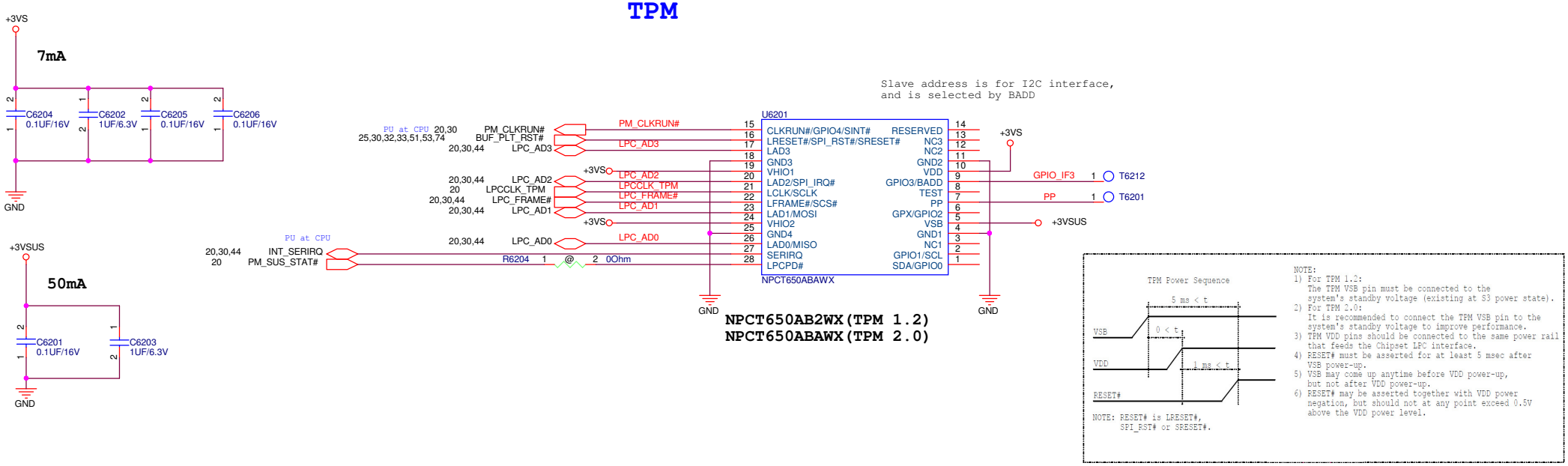
PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3 Engineer: Bill Yang

| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 1.0 |

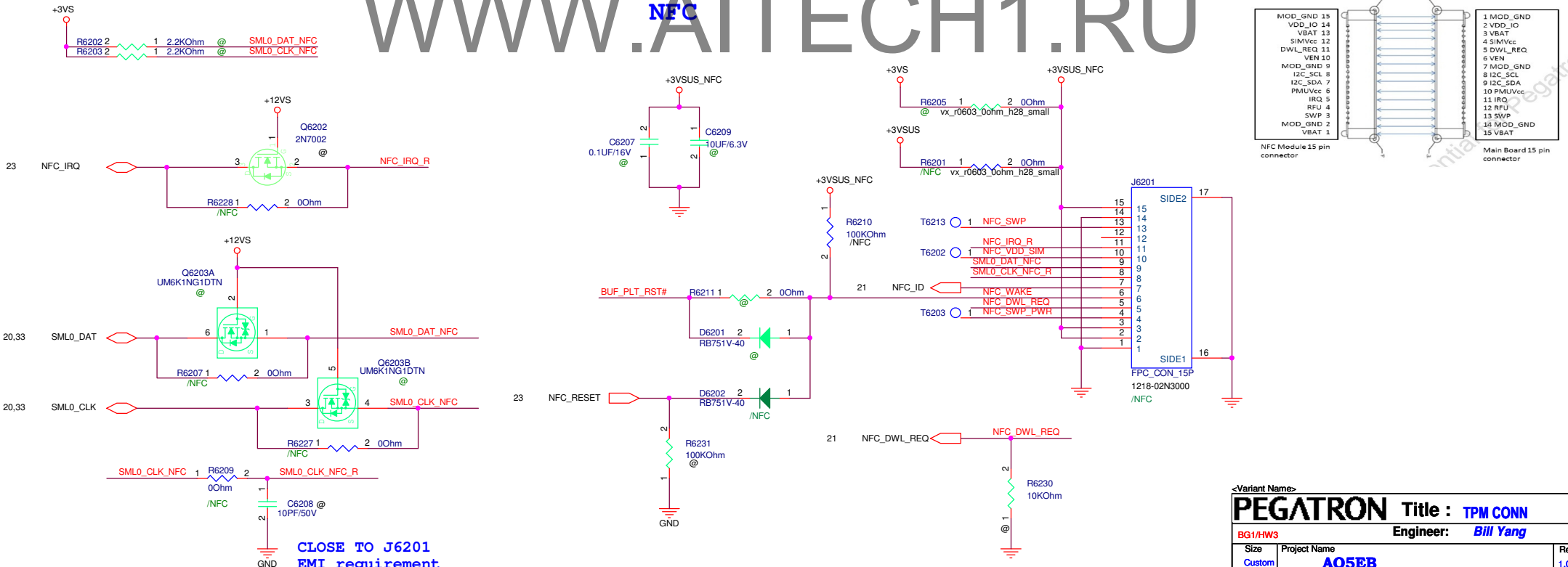
Date: Wednesday, August 23, 2017 Sheet 61 of 108

# TPM






# NFC




<Variant Name>

PEGATRON Title : TPM CONN

BG1/HW3 Engineer: Bill Yang

| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 1.0 |

Date: Wednesday, August 23, 2017 Sheet 62 of 108

| | | |
|---|---|---|
| Title | <Title> | |
| Size: A | Document Number: AQ5EB | Rev: 1.1 |
| Date: Wednesday, August 23, 2017 | Sheet 63 of 108 | |

| | | |
|---|---|---|
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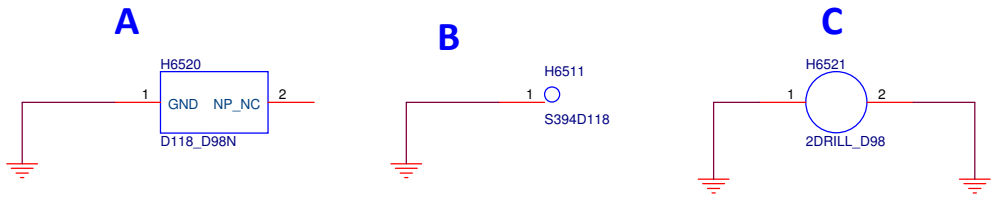
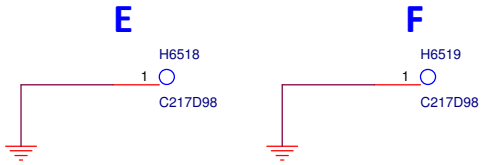
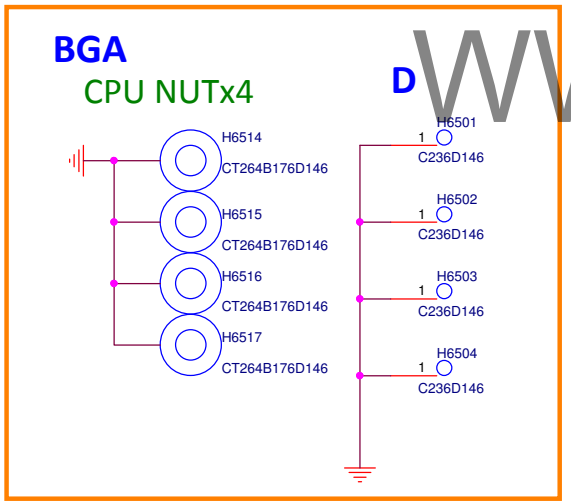
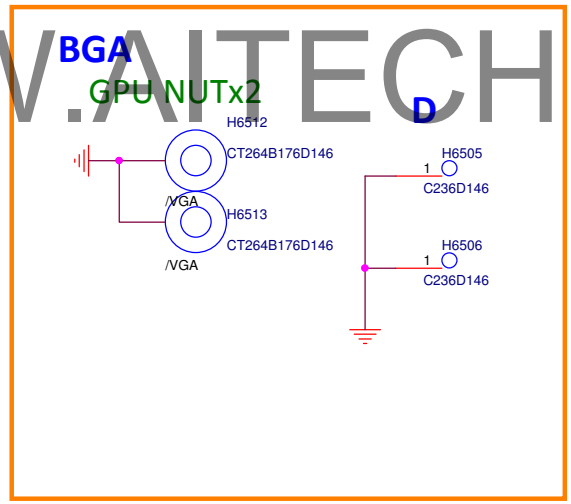
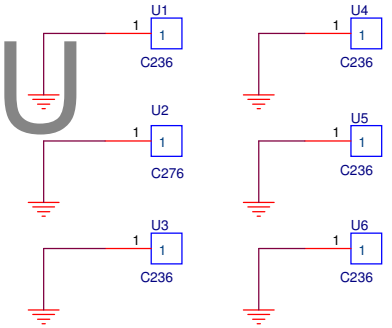
| Size A | Document Number <Doc> | Rev <RevCode> |
| Date: Wednesday, August 23, 2017 | Sheet 64 of 108 | |






<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

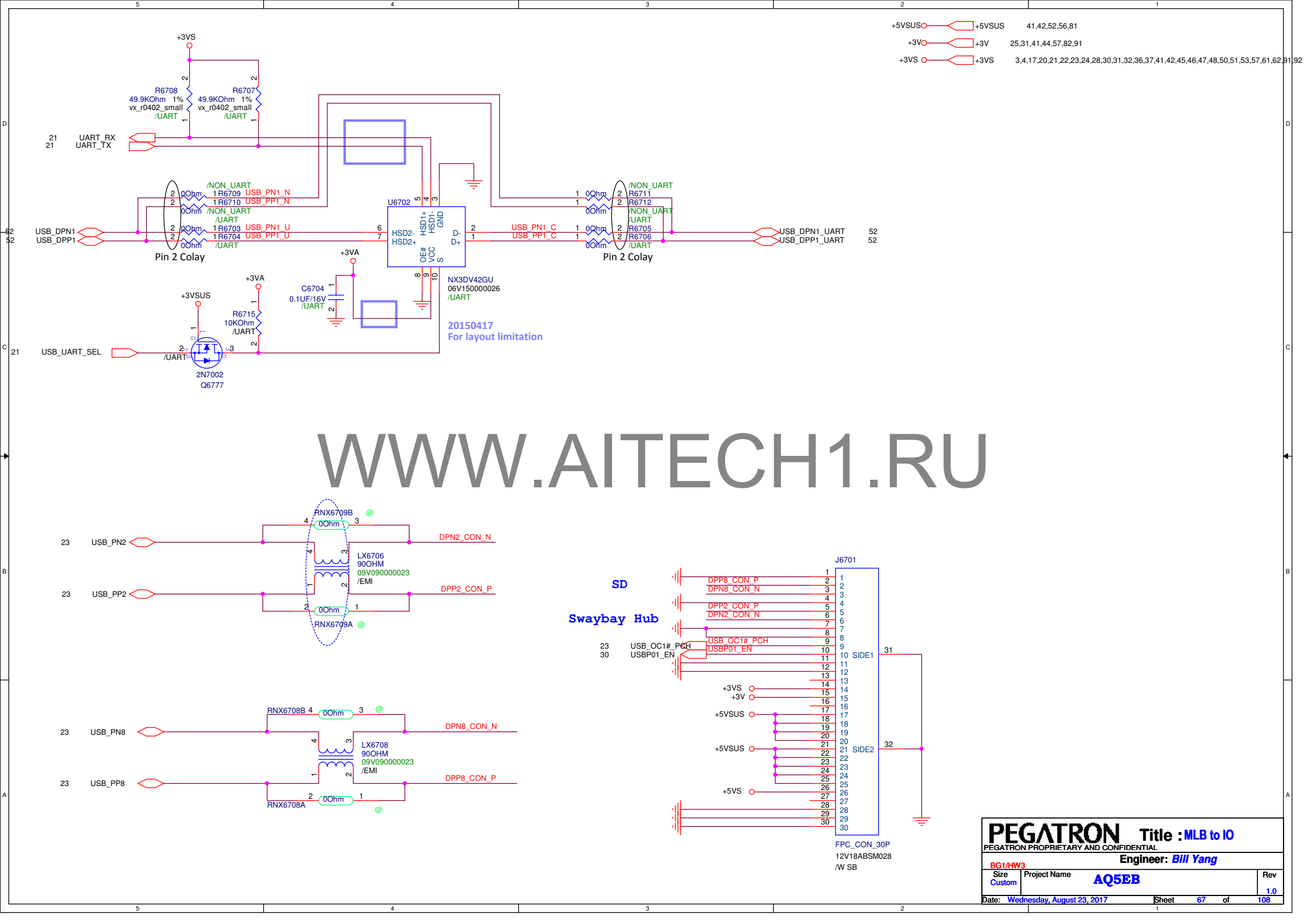
Title: ME_CONN,Skew Hole

Engineer: Bill Yang

| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 1.0 |

Date: Wednesday, August 23, 2017 Sheet 65 of 108

| | | |
|---|---|---|
| Title | <Title> | |
| Size A | Document Number <Doc> | Rev <RevCode> |
| Date: Wednesday, August 23, 2017 | Sheet 66 of 108 | |




PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : MLB to IO

Engineer: Bill Yang

BG1/HW3

| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 1.0 |

Date: Wednesday, August 23, 2017 Sheet 67 of 108

+3VSUS +3VSUS 4,24,25,26,28,30,31,33,42,51,53,62,67,81,92

+3VA +3VA 24,30,31,36,43,53,56,57,67,81,88,93

25,30 PM_SUSB# R6801 1 2 0Ohm /BYPAS_EC SUSB_EC# 30,57,91,92

25,30 PM_SUSC# R6802 1 2 0Ohm /BYPAS_EC SUSC_EC# 30,57,91

For Intel power sequence requestment
ALL_SYS_PWRGD to Delay_ALL_SYS_PGD >2ms

Delay By EC(2ms+ EC processing time (3ms~33ms)

30 DE_ALL_SYS_PGD_EC R6809 1 2 0Ohm /BYPAS_EC

+3VSUS

U6802
1 A
2 B
3 GND
5 VCC
4 Y
Vcc=2~5.5
/BYPAS_EC

PM_SUSB#

For shut down Sequence

R6808 1 2
@ 100KOhm
10V240000005

C6804 1 2
0.1UF/16V
@

GND GND

DE_ALL_SYS_PGD_HW 30



30 SYS_PWROK_EC SP6802 1 2 SYS_PWROK_EC_G

+3VSUS

U6803
1 A
2 B
3 GND
5 VCC
4 Y
Vcc=2~5.5
/BYPAS_EC

PM_SUSB#

For shut down Sequence

R6806 1 2
@ 100KOhm
10V240000005

GND

R6804 1 2 0Ohm /BYPAS_EC SYS_PWROK 25,30

<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

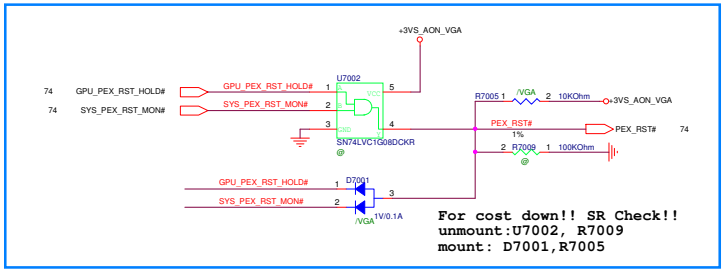
Title : BYPASS EC SEQUENCE

Engineer: Bill Yang

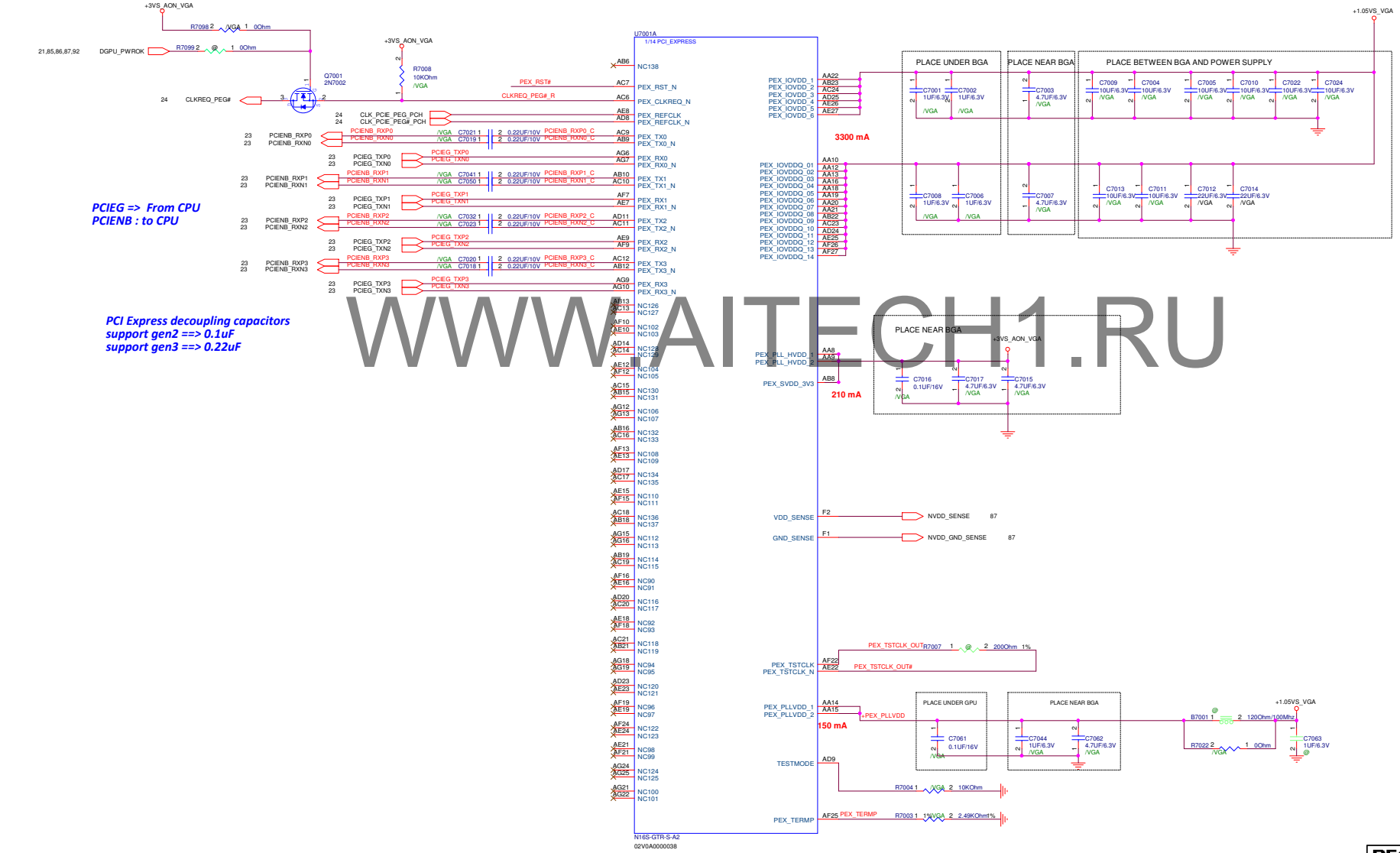
| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 1.0 |

Date: Wednesday, August 23, 2017 Sheet 68 of 108

| | | |
|---|---|---|
| Title <Title> | | |
| Size A | Document Number <Doc> | Rev <RevCode> |
| Date: Wednesday, August 23, 2017 | Sheet 69 of 108 | |

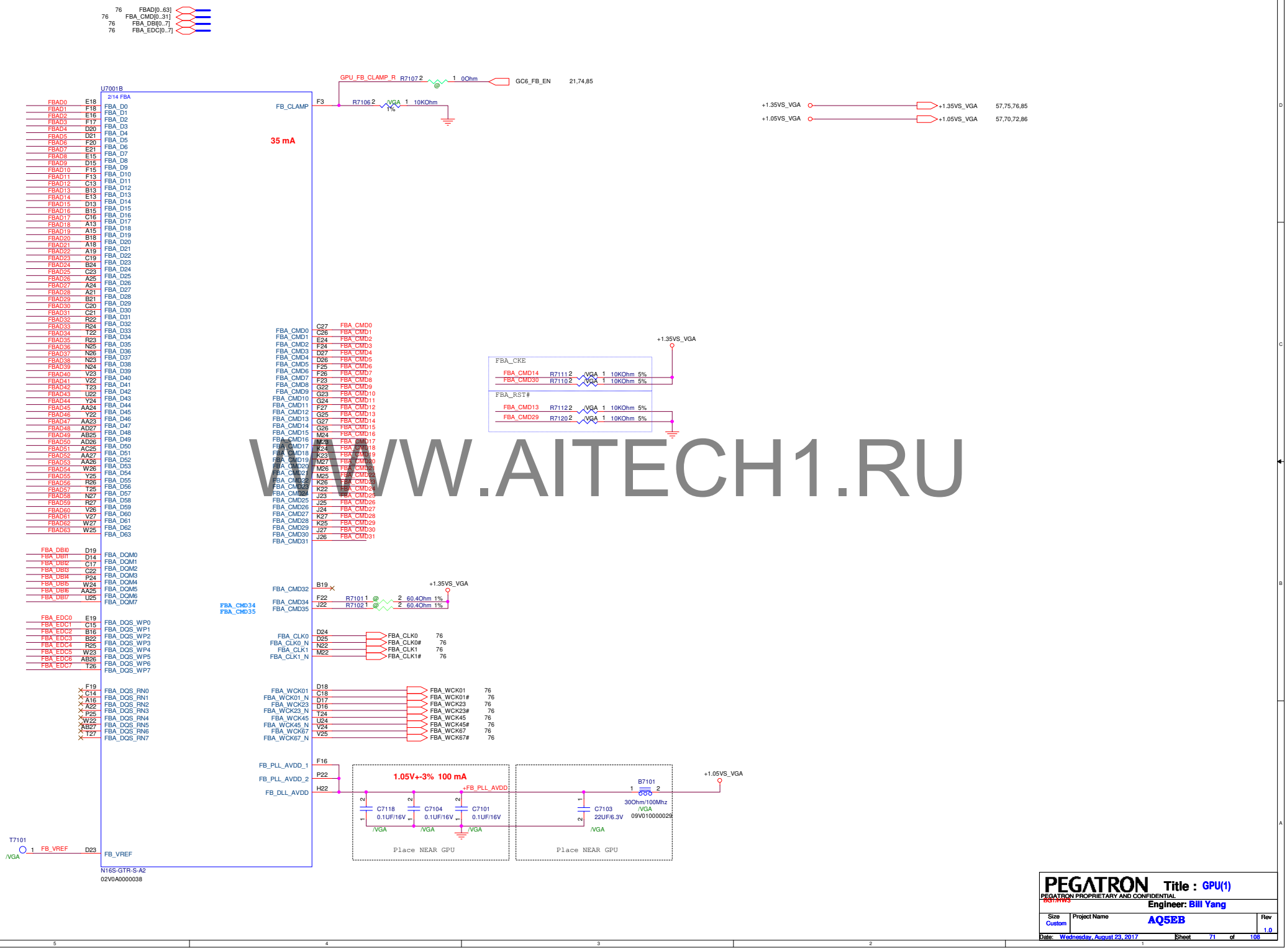









PEGATRON Title : GPU(1)
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Bill Yang
Size: Custom | Project Name: AQ5EB | Rev: 1.0
Date: Wednesday, August 23, 2017 | Sheet 70 of 108





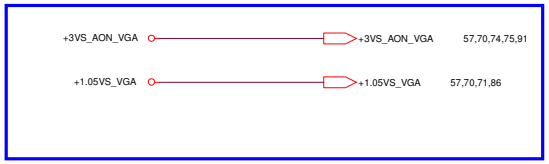

PEGATRON Title : GPU(1)

PEGATRON PROPRIETARY AND CONFIDENTIAL

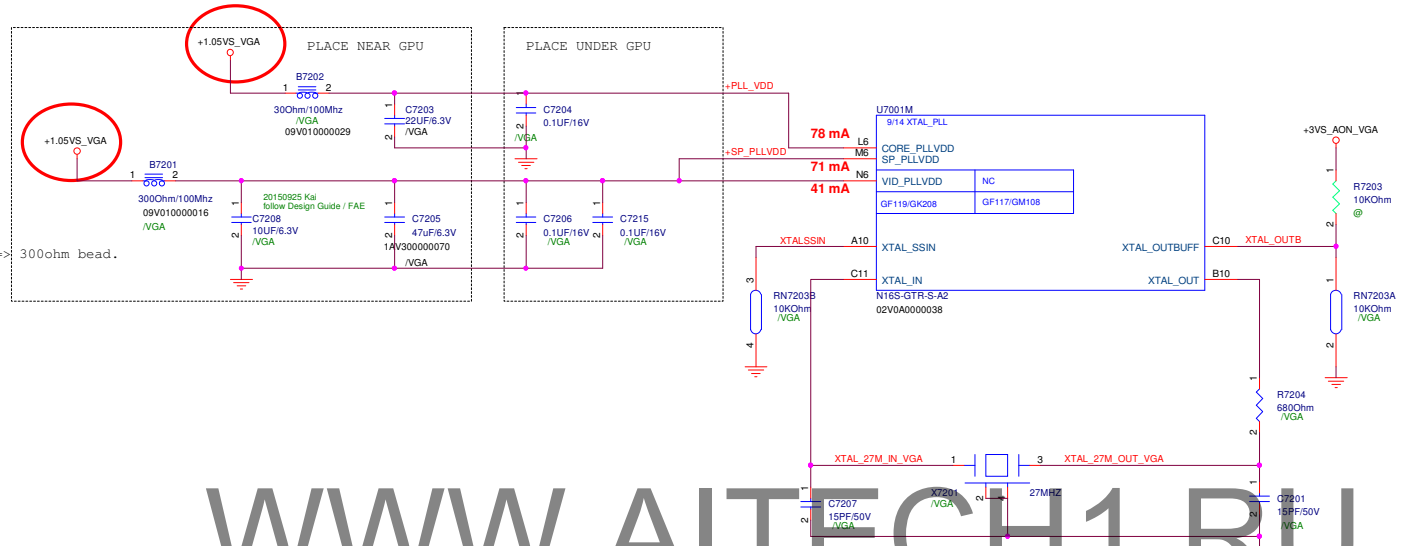
Engineer: Bill Yang

| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 1.0 |

Date: Wednesday, August 23, 2017 Sheet 71 of 108

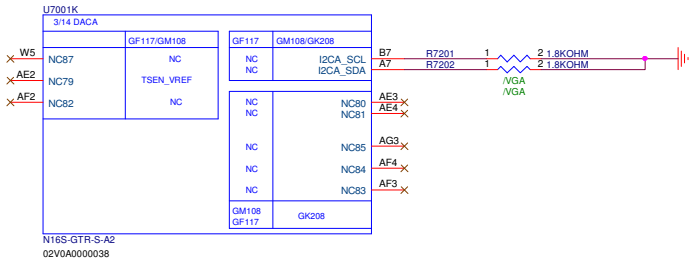



20141024 Chris




N16x series B7201==> 300ohm bead.






PEGATRON Title : GPU(1)

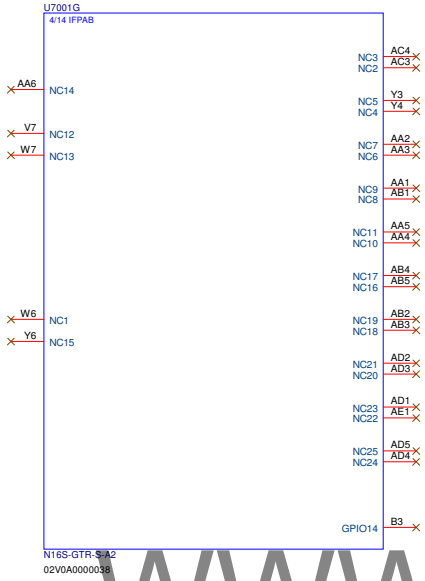
PEGATRON PROPRIETARY AND CONFIDENTIAL

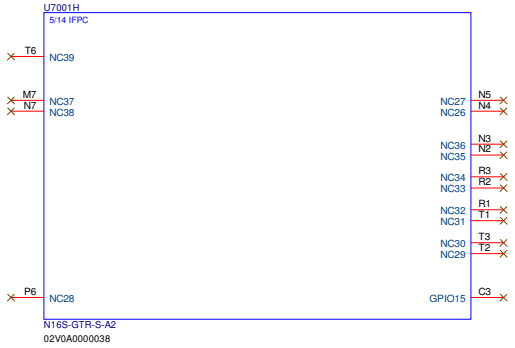
Engineer: Bill Yang

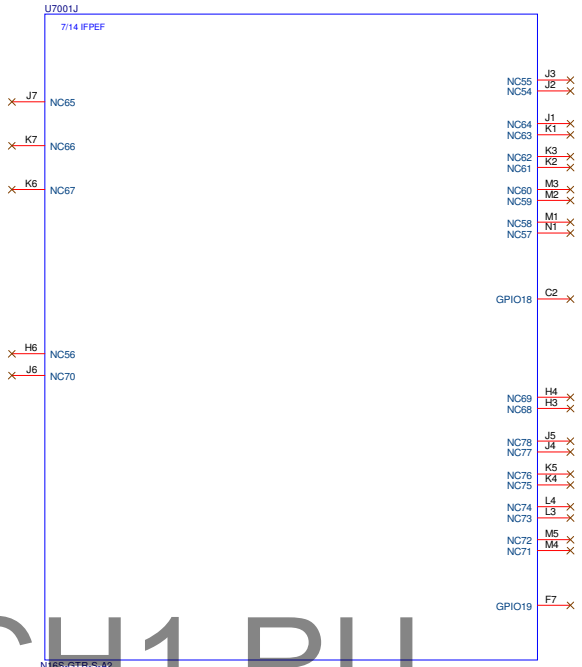
| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 1.0 |

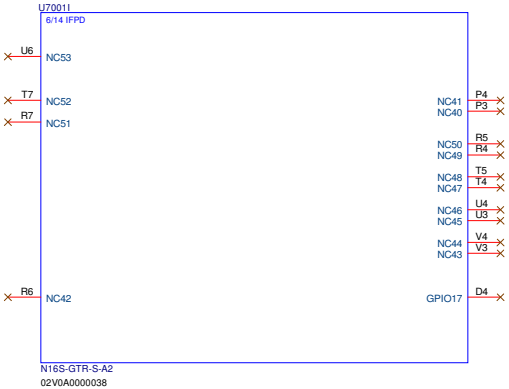
Date: Wednesday, August 23, 2017 Sheet 72 of 108

## LVDS






PEGATRON Title : GPU(1)

PEGATRON PROPRIETARY AND CONFIDENTIAL

BOM:HWS

Engineer: Bill Yang

| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 1.0 |

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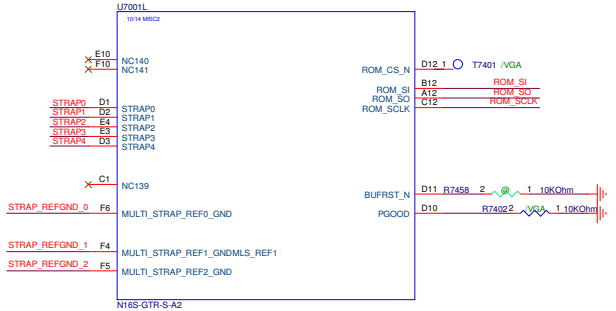
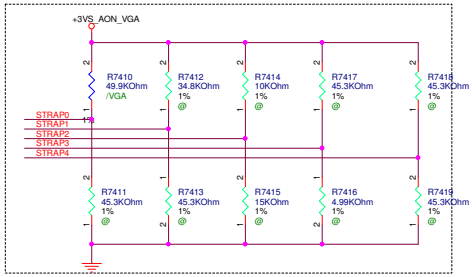
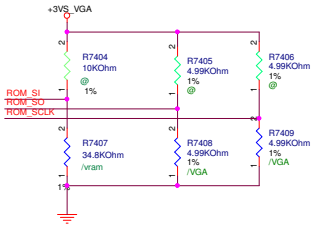
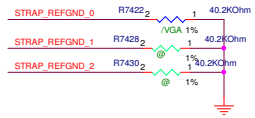
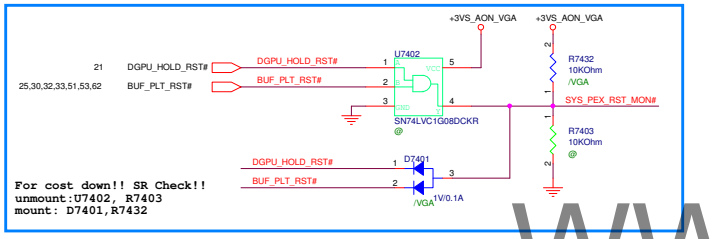


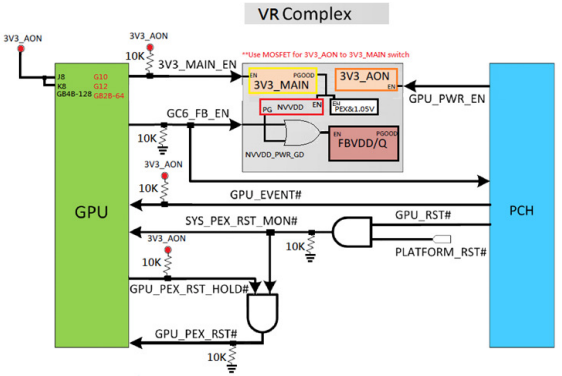





Strapping:

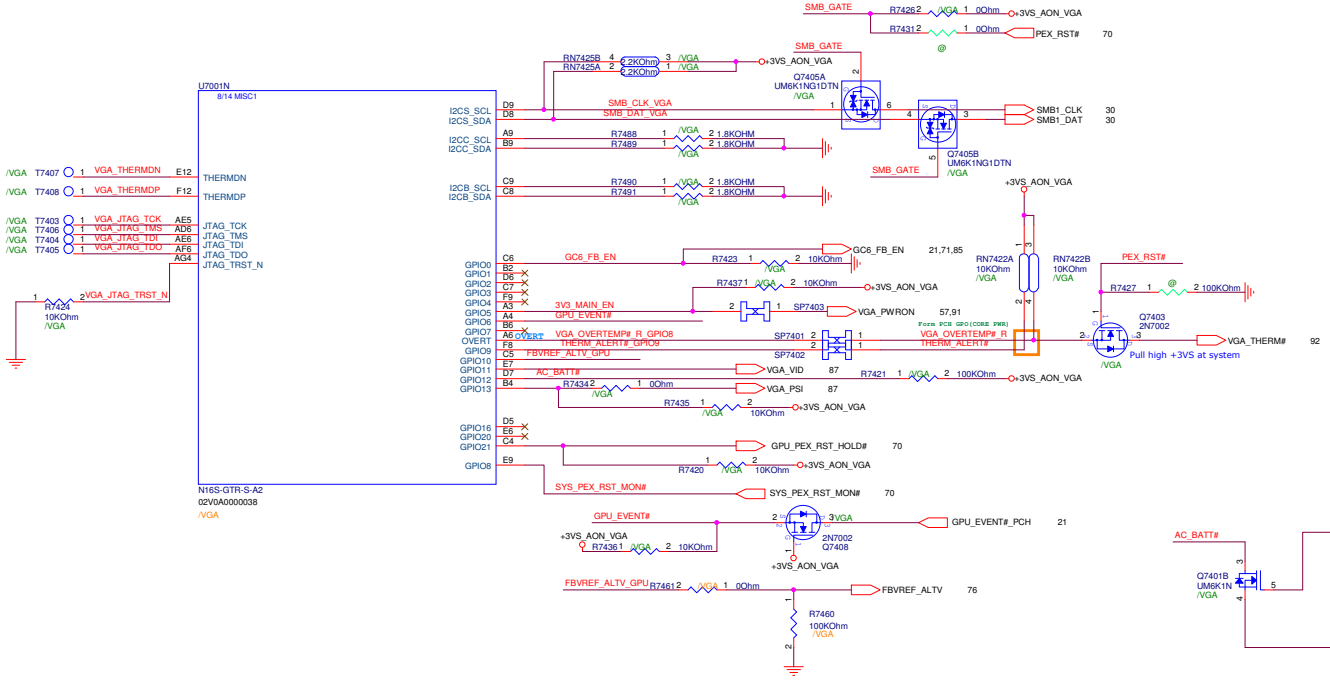
```
4.99K PU 1000 PD 0000
10.0K PU 1001 PD 0001
15.0K PU 1010 PD 0010
20.0K PU 1011 PD 0011
24.9K PU 1100 PD 0100
30.1K PU 1101 PD 0101
34.8K PU 1110 PD 0110
45.3K PU 1111 PD 0111


4.99K 10V220000077
10.0K 10V220000003
15.0K 10V220000023
20.0K 10V220000036
24.9K 10V220000049
30.1K 10V220000119
34.8K 10V220000061
45.3K 10V220000073
```

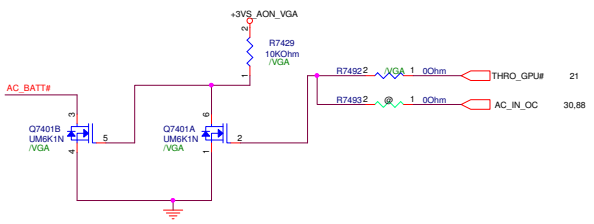
```
N16V-GTR

1.SAMSUNG: 0X0      (R7407 PD 5K  10V220000077)
2.MICRON:  0x1      (R7407 PD 10K 10V220000073)
```




GC6 2.0 High-level Signal Connections






| ROM_SI | | ROM_SO | | ROM_SCLK | |
|---|---|---|---|---|---|
| R7404 | R7407 | R7405 | R7408 | R7406 | R7409 |
| 20k | N | 4.99K | N | 4.99K | N |
| N | 45.3k | 4.99K | N | 4.99K | N |
| 34.8k | N | 4.99K | N | 4.99K | N |
| N | 30.1k | 4.99K | N | 4.99K | N |
| 10k | N | N | 4.99K | N | 4.99K |
| 20k | N | N | 4.99K | N | 4.99K |
| N | 20k | N | 4.99K | N | 4.99K |
| N | 30.1k | N | 4.99K | N | 4.99K |

PEGATRON Title : GPU(1)

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Bill Yang

| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 1.0 |

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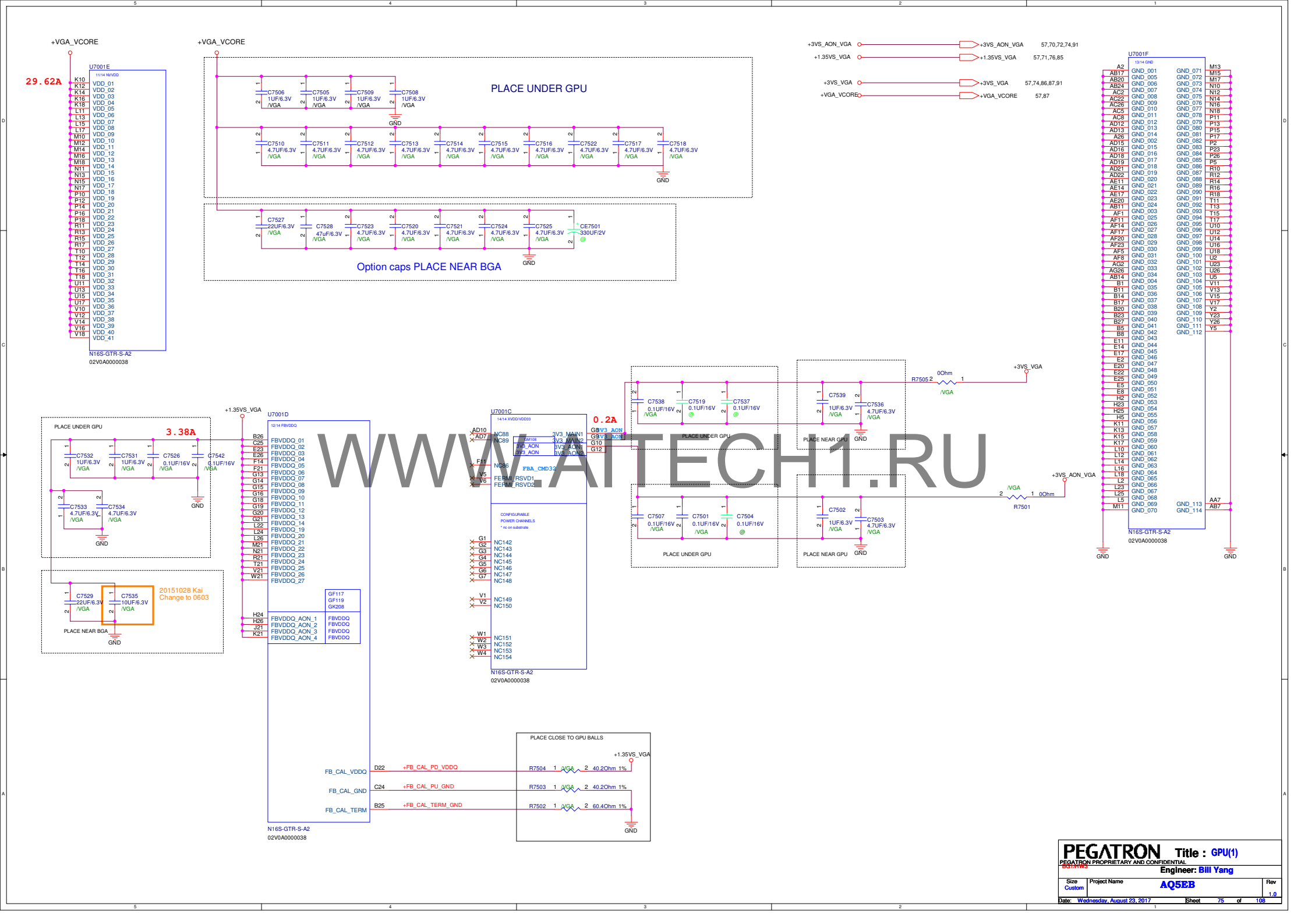
+VGA_VCORE
29.62A
U7001E
11/14 NVVDD
VDD_01
VDD_02
VDD_03
VDD_04
VDD_05
VDD_06
VDD_07
VDD_08
VDD_09
VDD_10
VDD_11
VDD_12
VDD_13
VDD_14
VDD_15
VDD_16
VDD_17
VDD_18
VDD_19
VDD_20
VDD_21
VDD_22
VDD_23
VDD_24
VDD_25
VDD_26
VDD_27
VDD_28
VDD_29
VDD_30
VDD_31
VDD_32
VDD_33
VDD_34
VDD_35
VDD_36
VDD_37
VDD_38
VDD_39
VDD_40
VDD_41
N16S-GTR-S-A2
02V0A0000038
PLACE UNDER GPU
C7506 1UF/6.3V /VGA
C7505 1UF/6.3V /VGA
C7509 1UF/6.3V /VGA
C7508 1UF/6.3V /VGA
C7510 4.7UF/6.3V /VGA
C7511 4.7UF/6.3V /VGA
C7512 4.7UF/6.3V /VGA
C7513 4.7UF/6.3V /VGA
C7514 4.7UF/6.3V /VGA
C7515 4.7UF/6.3V /VGA
C7516 4.7UF/6.3V /VGA
C7522 4.7UF/6.3V /VGA
C7517 4.7UF/6.3V /VGA
C7518 4.7UF/6.3V /VGA
GND
Option caps PLACE NEAR BGA
C7527 22UF/6.3V /VGA
C7528 47uF/6.3V /VGA
C7523 4.7UF/6.3V /VGA
C7520 4.7UF/6.3V /VGA
C7521 4.7UF/6.3V /VGA
C7524 4.7UF/6.3V /VGA
C7525 4.7UF/6.3V /VGA
CE7501 330UF/2V @
+3VS_AON_VGA
+1.35VS_VGA
+3VS_VGA
+VGA_VCORE
+3VS_AON_VGA 57,70,72,74,91
+1.35VS_VGA 57,71,76,85
+3VS_VGA 57,74,86,87,91
+VGA_VCORE 57,87
U7001F
13/14 GND
N16S-GTR-S-A2
02V0A0000038
+1.35VS_VGA
U7001D
12/14 FBVDDQ
PLACE UNDER GPU
3.38A
C7532 1UF/6.3V /VGA
C7531 1UF/6.3V /VGA
C7526 0.1UF/16V /VGA
C7542 0.1UF/16V /VGA
C7533 4.7UF/6.3V /VGA
C7534 4.7UF/6.3V /VGA
GND
PLACE NEAR BGA
C7529 22UF/6.3V /VGA
C7535 10UF/6.3V /VGA
20151028 Kai Change to 0603
FBVDDQ_01
FBVDDQ_02
FBVDDQ_03
FBVDDQ_04
FBVDDQ_05
FBVDDQ_06
FBVDDQ_07
FBVDDQ_08
FBVDDQ_09
FBVDDQ_10
FBVDDQ_11
FBVDDQ_12
FBVDDQ_13
FBVDDQ_14
FBVDDQ_19
FBVDDQ_20
FBVDDQ_21
FBVDDQ_22
FBVDDQ_23
FBVDDQ_24
FBVDDQ_25
FBVDDQ_26
FBVDDQ_27
FBVDDQ_AON_1
FBVDDQ_AON_2
FBVDDQ_AON_3
FBVDDQ_AON_4
GF117
GF119
GK208
FBVDDQ
N16S-GTR-S-A2
02V0A0000038
U7001C
14/14 XVDD/VDD33
0.2A
3V3_MAIN1
3V3_MAIN2
3V3_AON
3V3_AON
3V3_AON1
3V3_AON2
FBA_CMD32
FERMI_RSVD1
FERMI_RSVD2
CONFIGURABLE POWER CHANNELS
* nc on substrate
NC142
NC143
NC144
NC145
NC146
NC147
NC148
NC149
NC150
NC151
NC152
NC153
NC154
N16S-GTR-S-A2
02V0A0000038
C7538 0.1UF/16V /VGA
C7519 0.1UF/16V @
C7537 0.1UF/16V @
C7539 1UF/6.3V /VGA
C7536 4.7UF/6.3V /VGA
PLACE UNDER GPU
PLACE NEAR GPU
R7505 0Ohm /VGA
+3VS_VGA
C7507 0.1UF/16V /VGA
C7501 0.1UF/16V /VGA
C7504 0.1UF/16V @
C7502 1UF/6.3V /VGA
C7503 4.7UF/6.3V /VGA
+3VS_AON_VGA
R7501 /VGA 0Ohm
PLACE CLOSE TO GPU BALLS
+1.35VS_VGA
FB_CAL_VDDQ
FB_CAL_GND
FB_CAL_TERM
D22 +FB_CAL_PD_VDDQ
C24 +FB_CAL_PU_GND
B25 +FB_CAL_TERM_GND
R7504 /VGA 40.2Ohm 1%
R7503 /VGA 40.2Ohm 1%
R7502 /VGA 60.4Ohm 1%
GND
WWW.ATECH1.RU
PEGATRON
Title : GPU(1)
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Bill Yang
Size Custom
Project Name AQ5EB
Rev 1.0
Date: Wednesday, August 23, 2017
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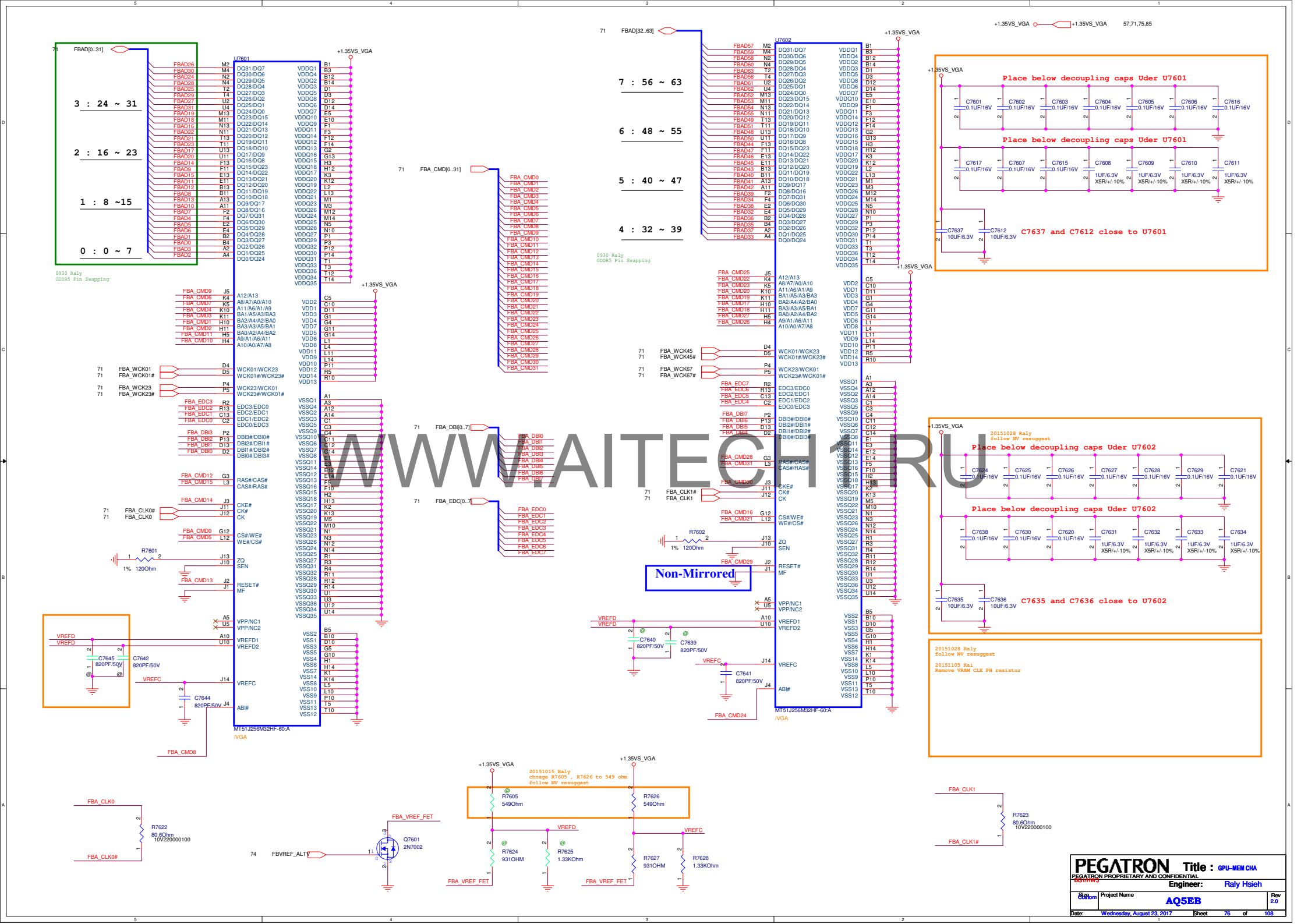


| | | |
|---|---|---|
| Title | <Title> | |
| Size A | Document Number <Doc> | Rev <RevCode> |
| Date: Wednesday, August 23, 2017 | Sheet 77 of 108 | |

PEGATRON Title : ****

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3 Engineer: *Raly Hsieh*

| Size | Project Name | Rev |
|---|---|---|
| A | **AQ5EB** | 1.0 |

Date: Wednesday, August 23, 2017 Sheet 78 of 99

PEGATRON Title : ****

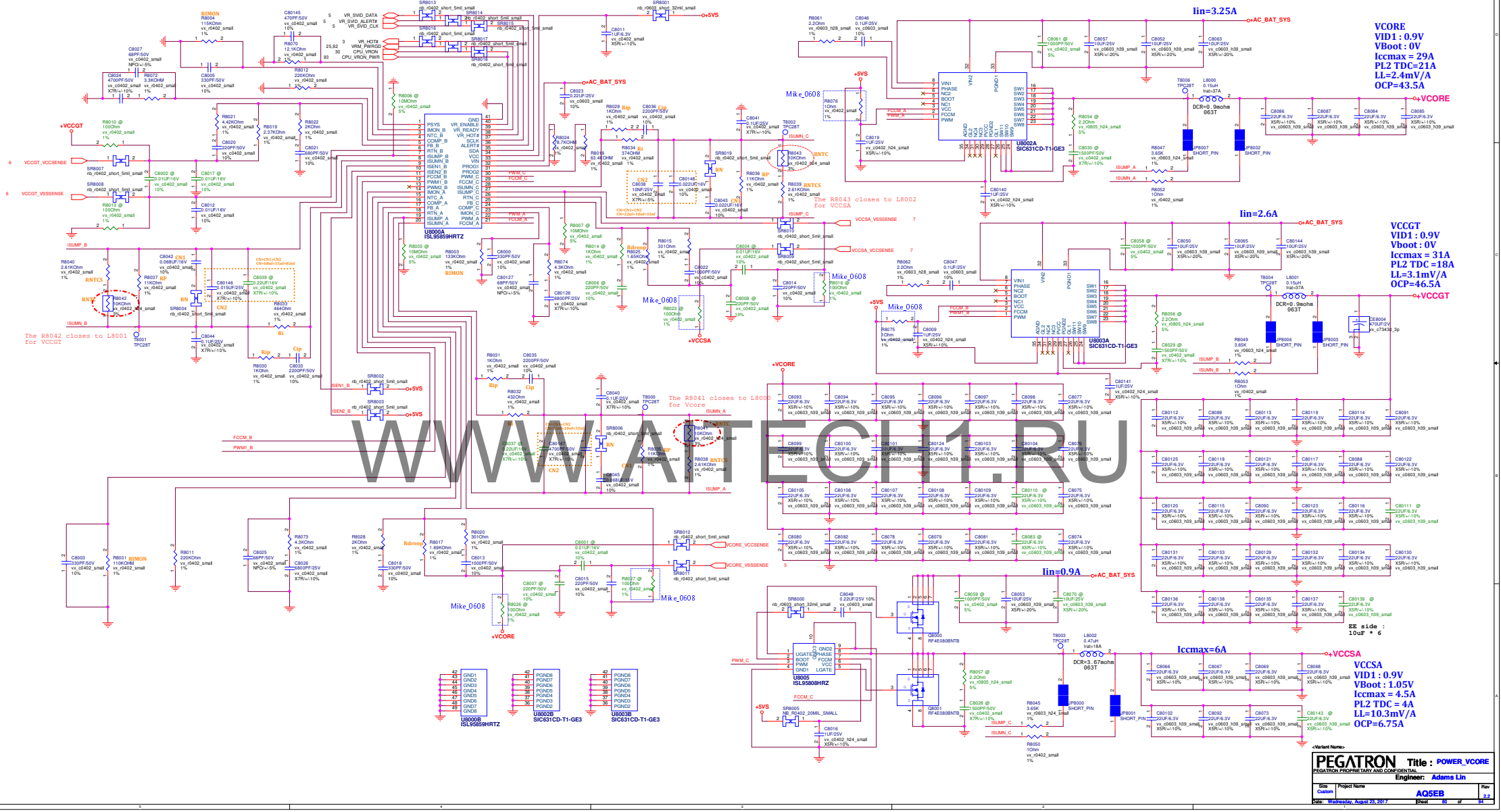
PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3 Engineer: *Raly Hsieh*

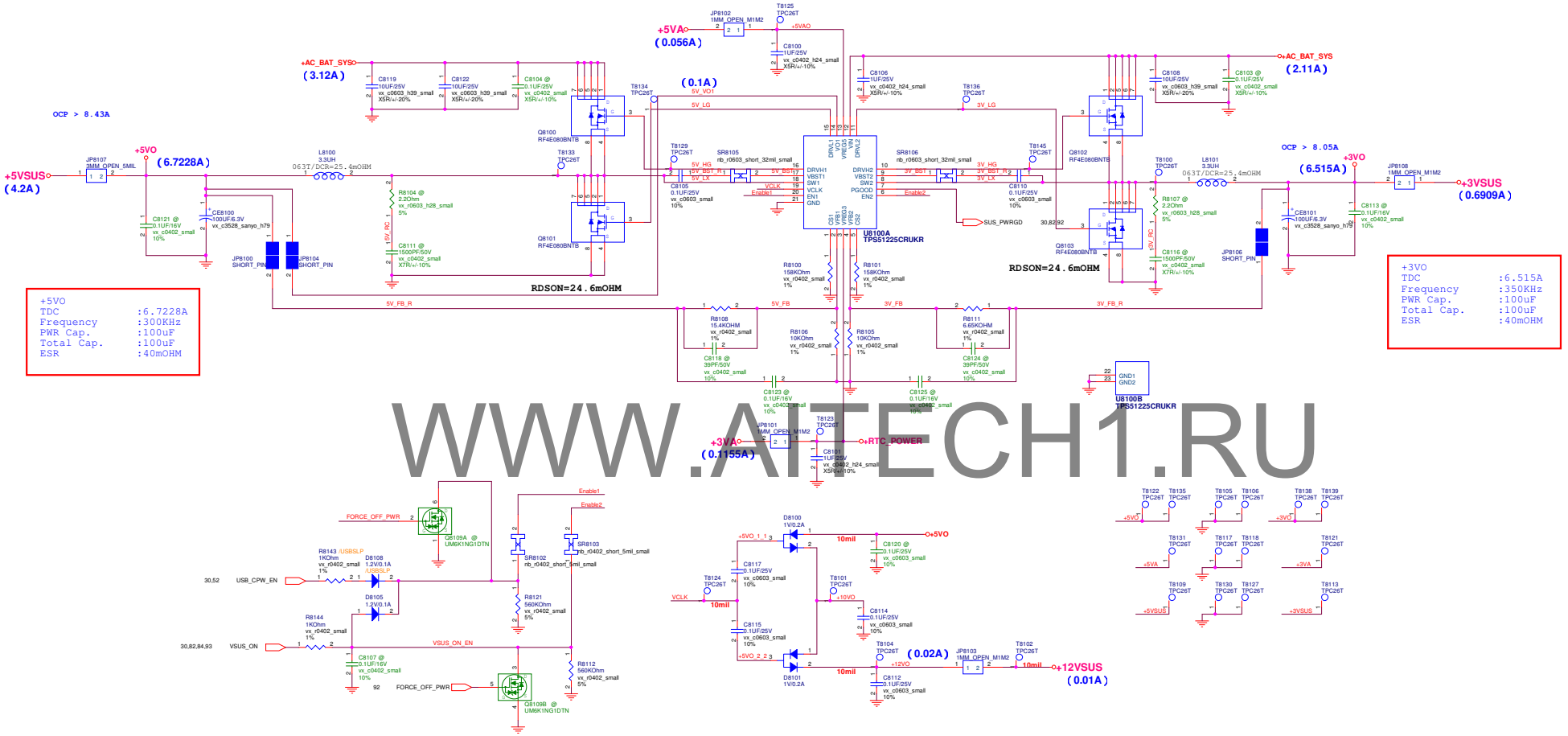
| Size | Project Name | Rev |
|---|---|---|
| A | **AQ5EB** | 1.0 |

Date: Wednesday, August 23, 2017 Sheet 79 of 99

# VCORE & VCCGT & VCCSA POWER SUPPLY



# 5VO & 3VO POWER SUPPLY






PEGATRON Title : POWER_SYSTEM

PEGATRON PROPRIETARY AND CONFIDENTIAL

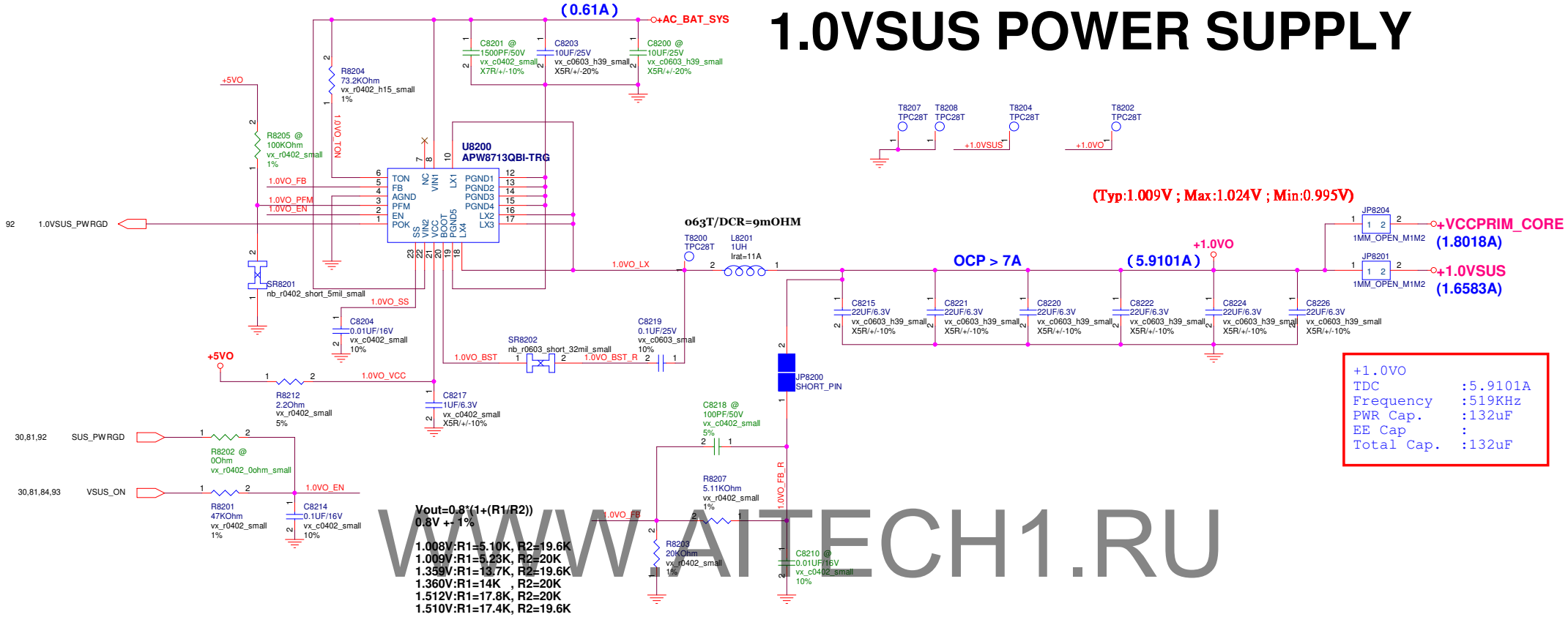
Engineer: Adams Lin

BG1-POWER

Size: Custom | Project Name: AQ5EB | Rev: 0.2

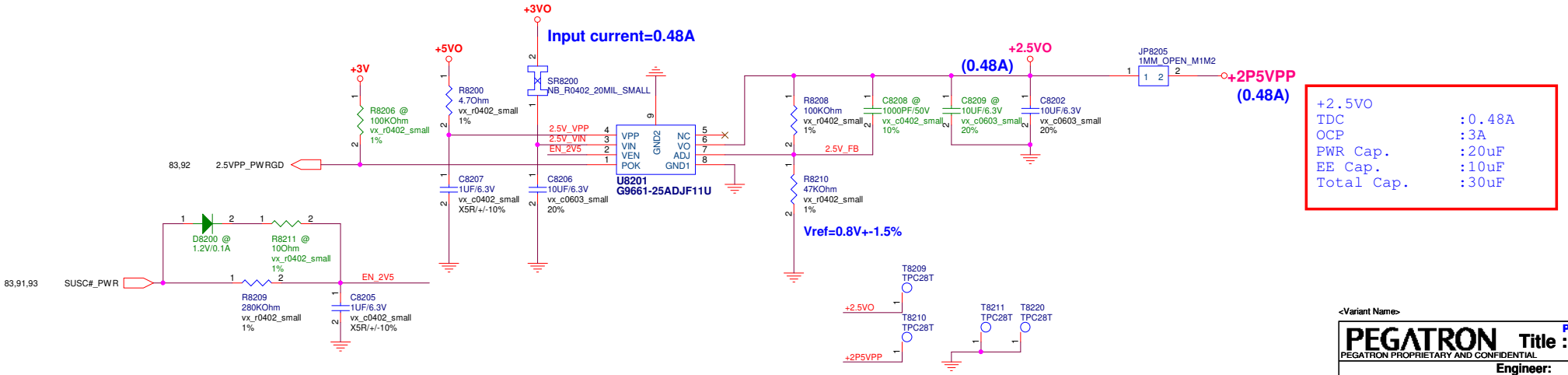
Date: Wednesday, August 23, 2017 | Sheet 81 of 94

# 1.0VSUS POWER SUPPLY

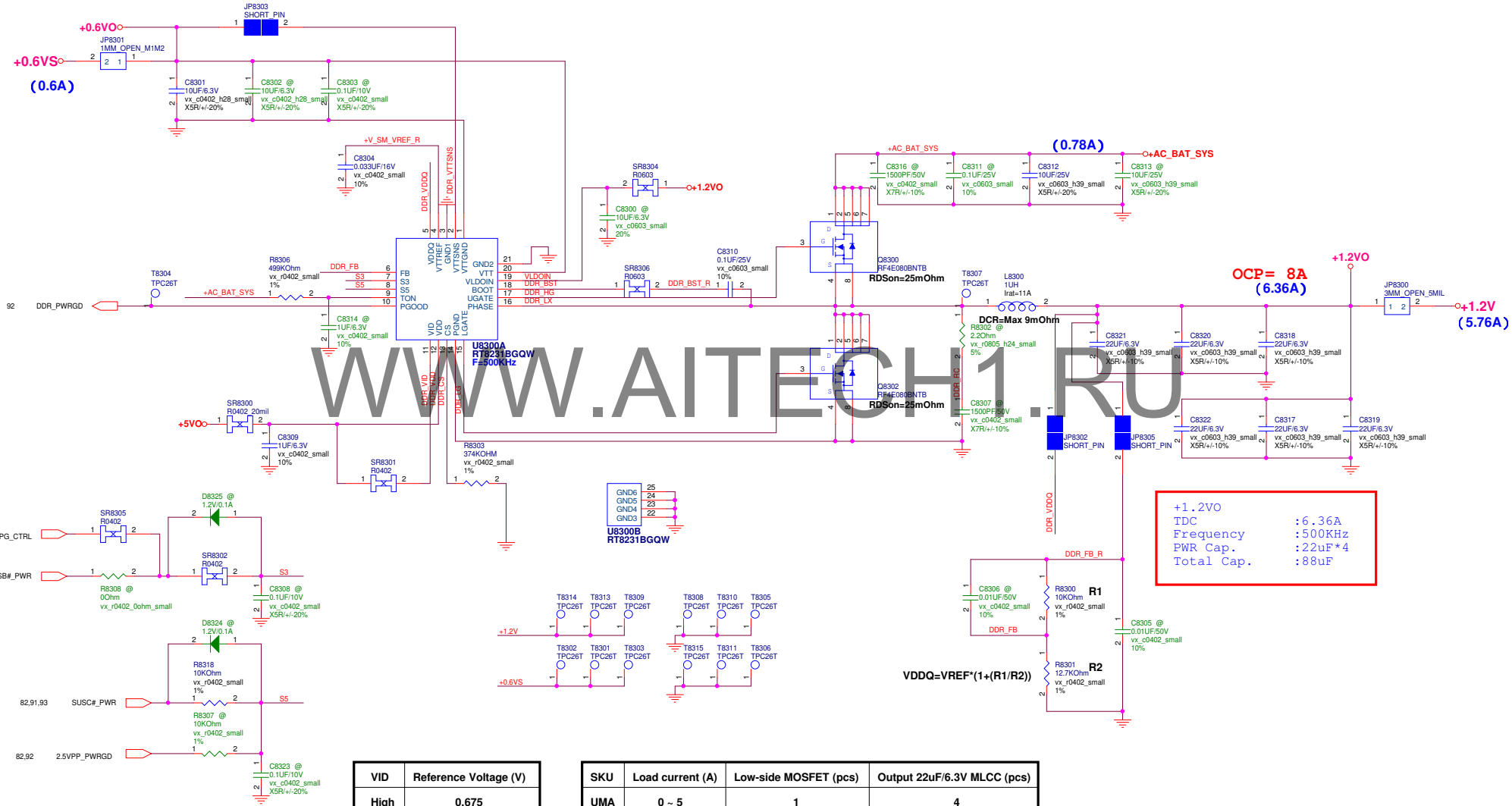





# 2.5V POWER SUPPLY



# DDR & VTT POWER SUPPLY





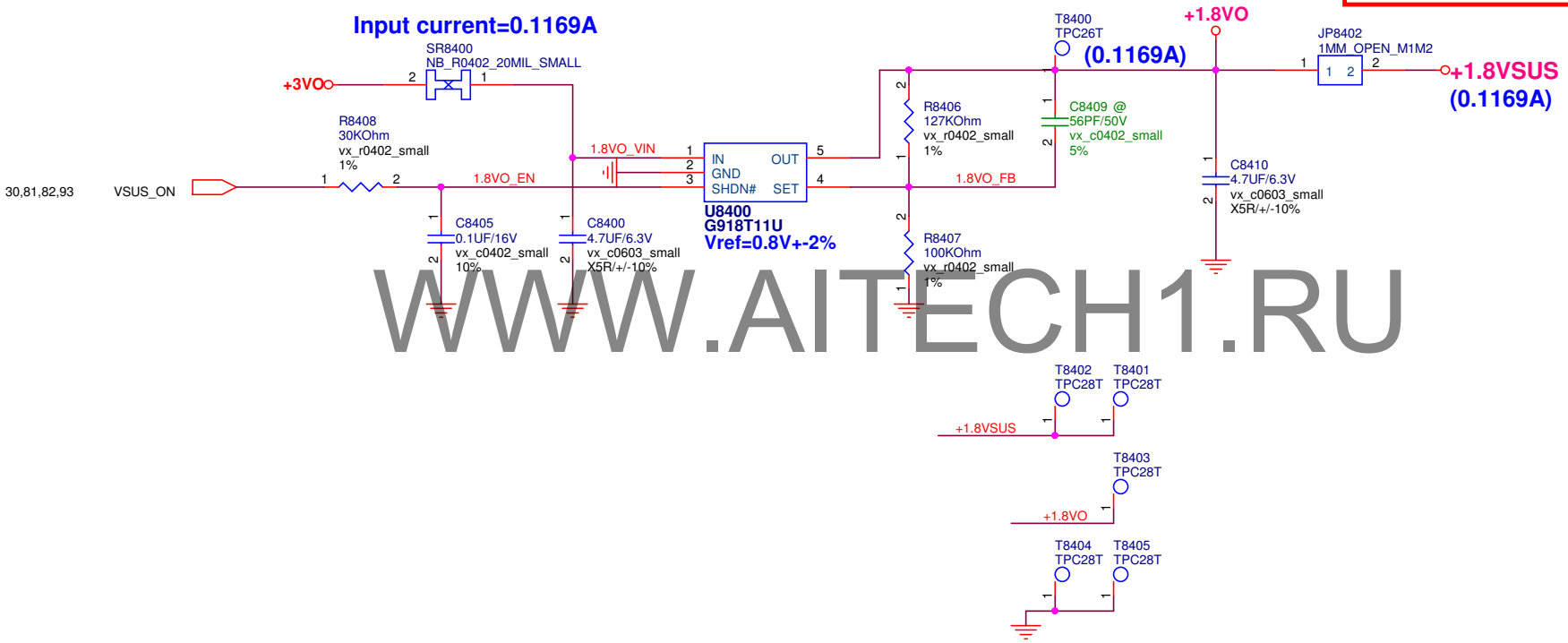

| VID | Reference Voltage (V) |
|---|---|
| High | 0.675 |
| Low | 0.75 |

| SKU | Load current (A) | Low-side MOSFET (pcs) | Output 22uF/6.3V MLCC (pcs) |
|---|---|---|---|
| UMA | 0 ~ 5 | 1 | 4 |
| DSC | 0 ~ 8 | 2 | 5 |

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : POWER_DDR & VTT
Engineer: Adams Lin
BG1-POWER
Size: Custom | Project Name: AQ5EB | Rev: 2.2
Date: Wednesday, August 23, 2017 | Sheet 83 of 94

# 1.8VSUS POWER SUPPLY

+1.8VO
MAX current :0.1169A
PWR Cap. :20uF
Total Cap. :20uF






<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

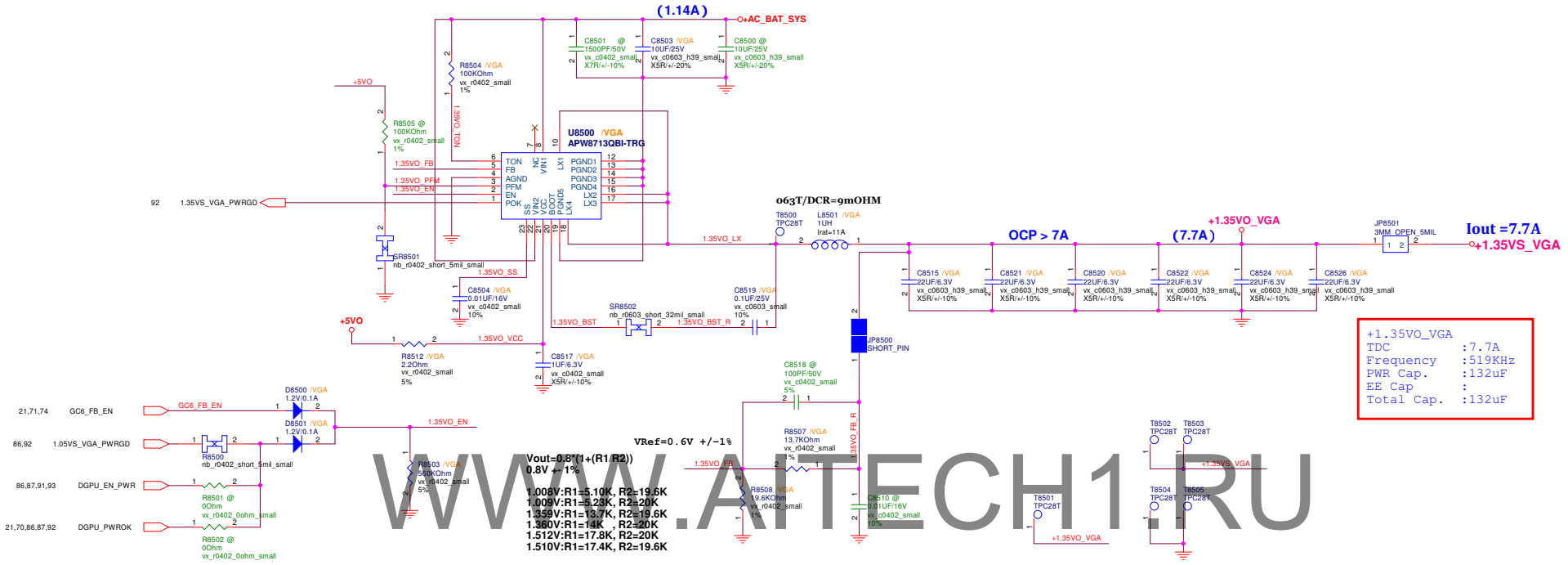
Title : POWER_+1.8VSUS

Engineer: Adams Lin

| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 2.2 |

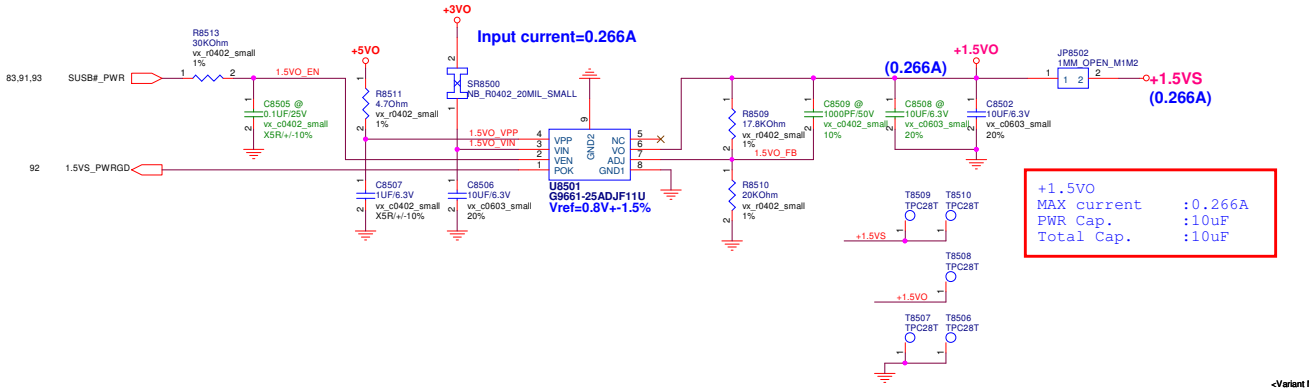
Date: Wednesday, August 23, 2017 Sheet 84 of 94

# 1.35VS_VGA POWER SUPPLY

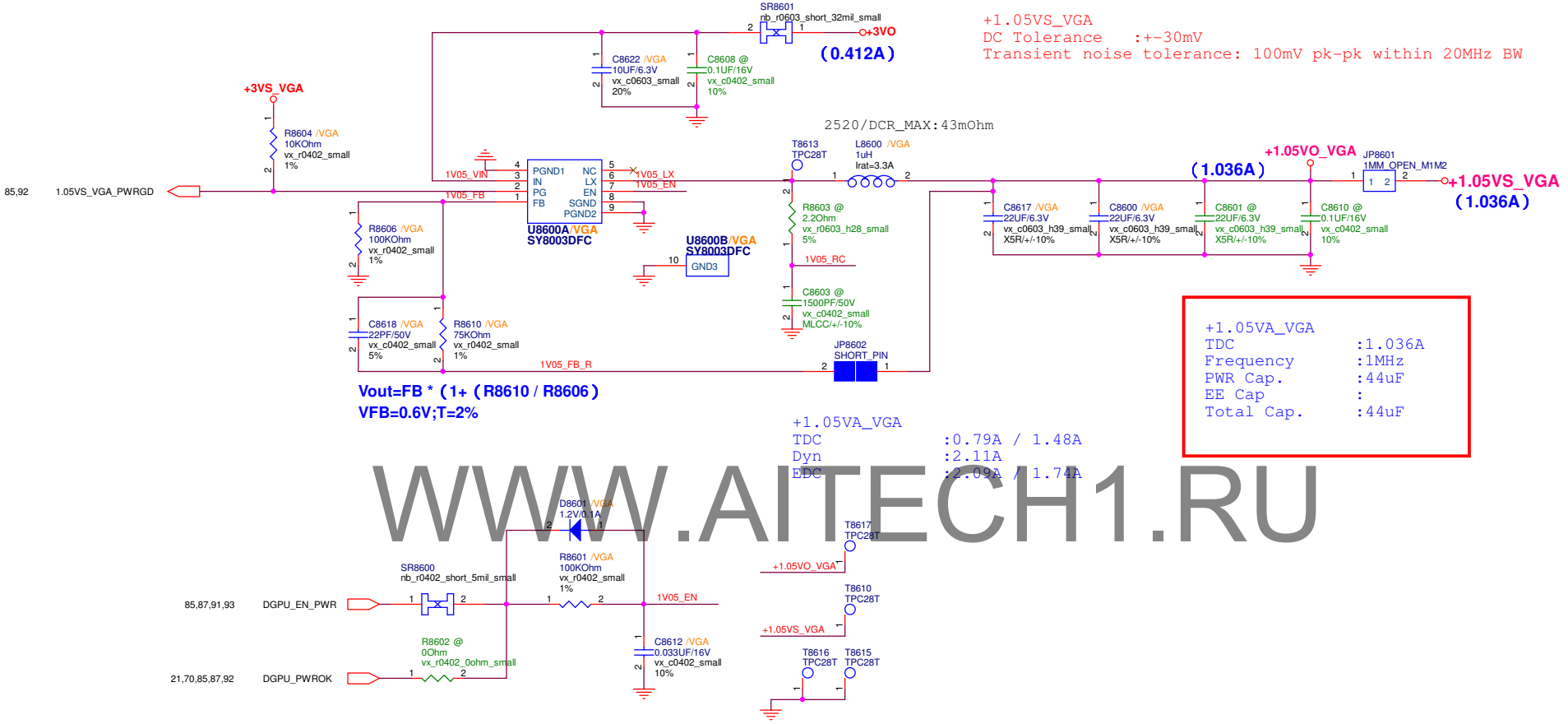





# 1.5VS POWER SUPPLY



# 1.05VS_VGA POWER SUPPLY






<Variant Name>

PEGATRON Title : +1.05VS_VGA

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Adams Lin

| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 2.2 |

Date: Wednesday, August 23, 2017 Sheet 86 of 94

# VGA_CORE POWER SUPPLY

+VGA_VCORE(Package type:N16VS-GT)
DC Tolerance :+-20mV

Overshoot/undershoot
Transient noise tolerance: -10% ~ +20% within 20MHz BW
High frequency noise: 400mV pk-pk within 1GHz BW

VID:0.6V ~ 1.2V
Number of programmable Volt: 96 levels
Programmable volt steps: 6.25mV
Settling Time: < 100us for rising, no restriction on falling

| | N16 | N16S_GT |
|---|---|---|
| R8723 | 39K | 20K |
| R8721 | 39K | 20K |
| R8716 | 1.5K | 2K |
| R8713 | 31.5K | 18K |
| C8720 | >1.8nF | 2.7nF |
| Vstep | 6.25mV | 6.25mV |
| Vmin | 0.65V | 0.6V |
| Vmax | 1.15V | 1.2V |
| Vboot | 0.875V | 0.9V |
| openVR Config | A | B |

| VGA_PSI# | VO_action |
|---|---|
| ~ 0.8V | 1 Phase DEM |
| 1.2 ~ 1.8V | 1 Phase FCCM |
| 2.4V ~ | 2 Phase FCCM |

2 PHASE 25W
N16S-GT
EDP=51A
TDC=26A
DYN= A
OCP:62A

+VGA_VCORE ( 2 Phase )
TDC :30A
Frequency :305KHz
PWR Cap. :940uF
EE Cap. :139.5uF
Total Cap. :1079.5uF
ESR :3mOHM

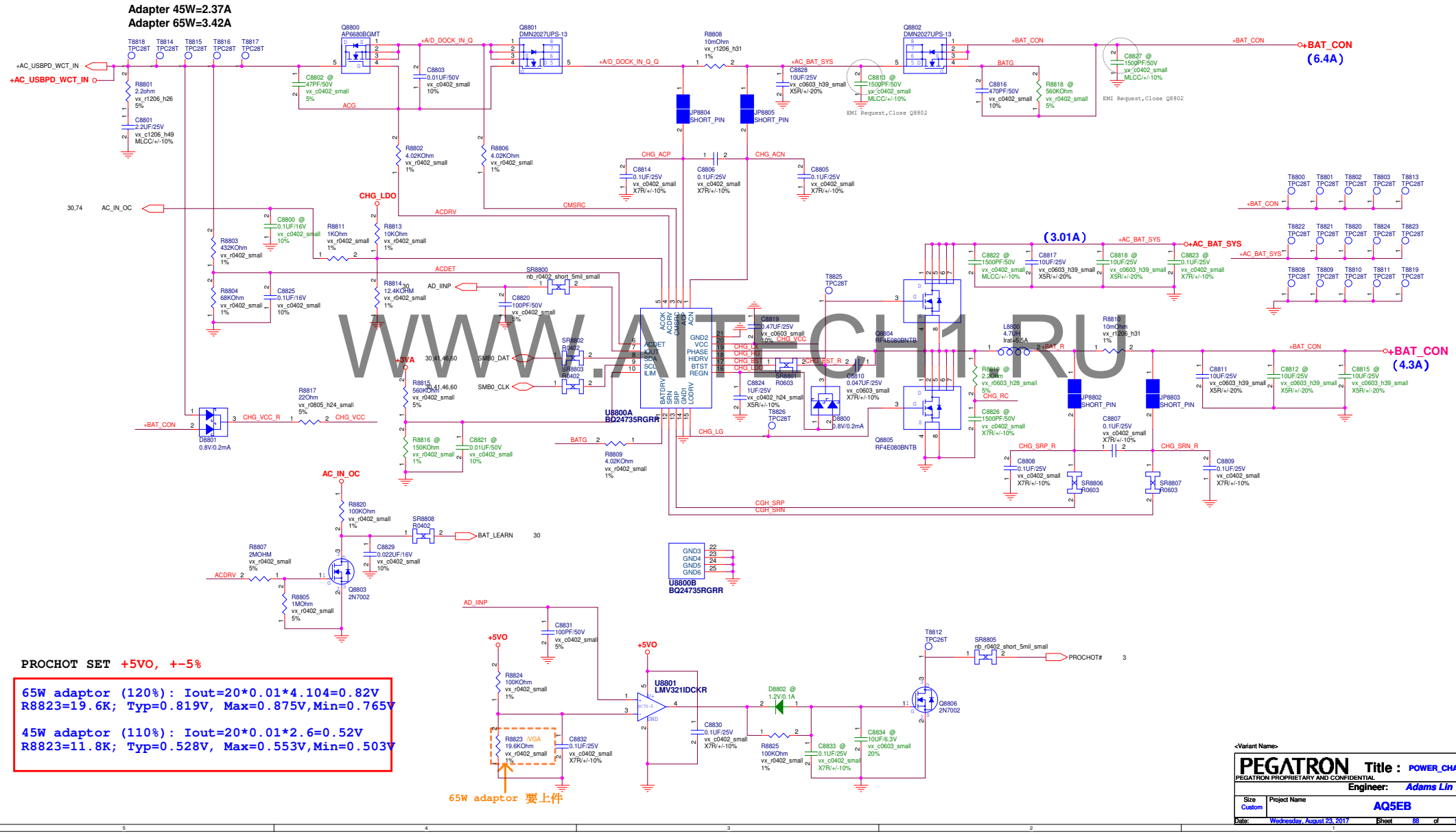
EE side pull high OHM check



<Variant Name>

PEGATRON Title : +VGA_VCORE
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Adams Lin
Size Custom | Project Name AQ5EB | Rev 2.2
Date: Wednesday, August 23, 2017 | Sheet 87 of 94

# BATTERY CHARGER




**PROCHOT SET +5VO, +-5%**

65W adaptor (120%): Iout=20*0.01*4.104=0.82V
R8823=19.6K; Typ=0.819V, Max=0.875V,Min=0.765V

45W adaptor (110%): Iout=20*0.01*2.6=0.52V
R8823=11.8K; Typ=0.528V, Max=0.553V,Min=0.503V



<Variant Name>

PEGATRON PROPRIETARY AND CONFIDENTIAL

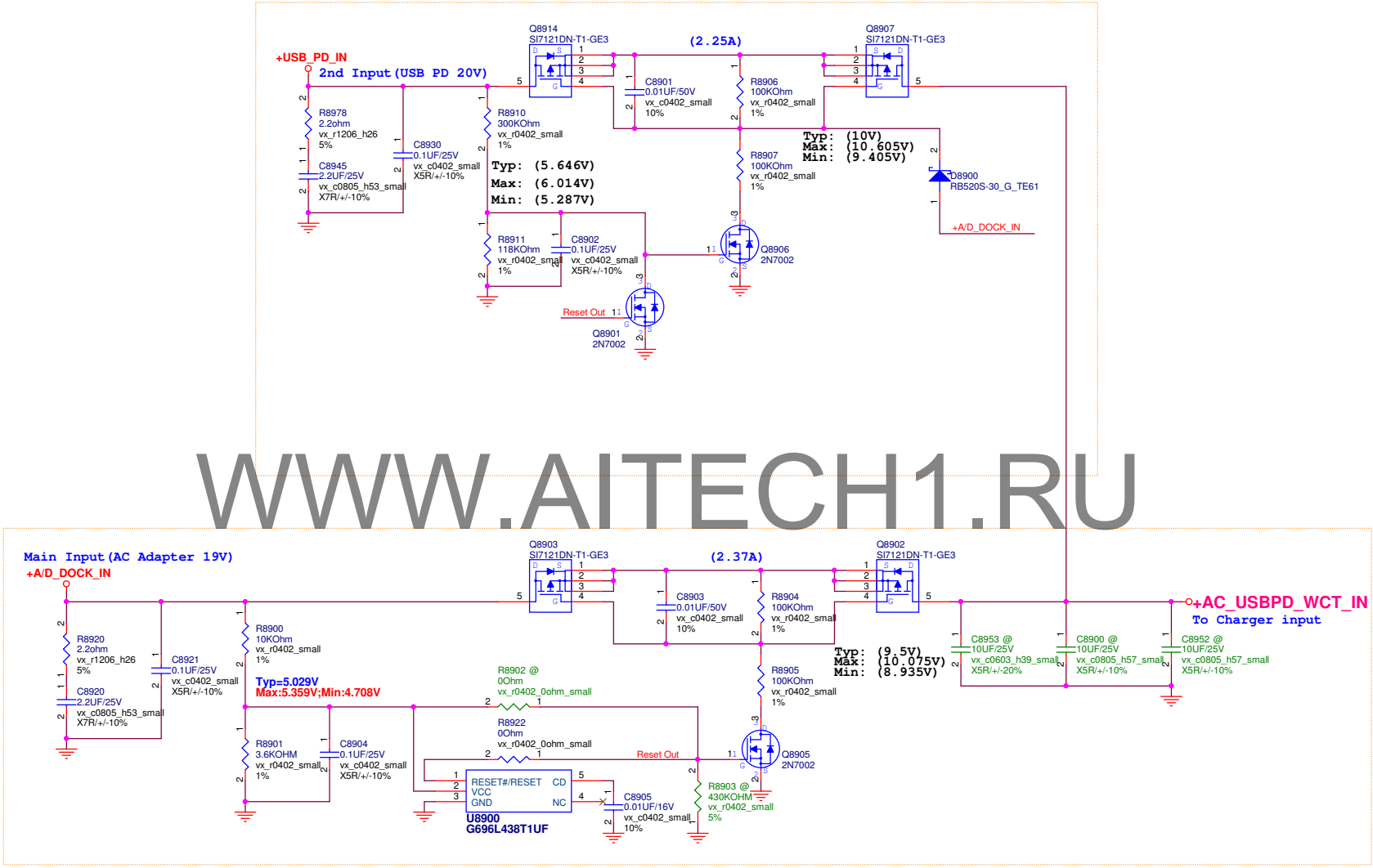
Title : POWER_CHARGER

Engineer: Adams Lin

| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 2.2 |

Date: Wednesday, August 23, 2017 Sheet 88 of 94

# 2 Input switch Circuit




PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

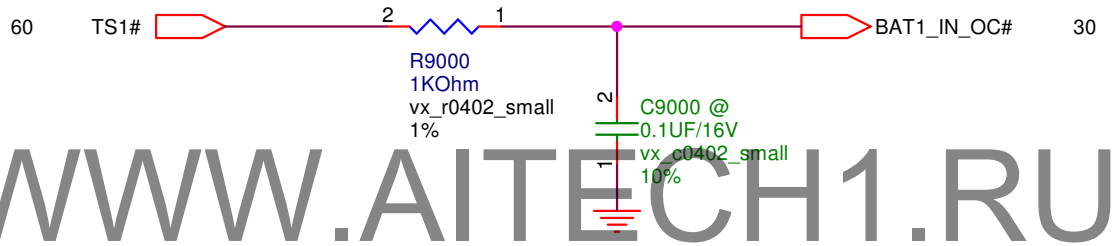
Title : AC&PD S.W.

Engineer: Adams Lin

| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 1.1 |

Date: Wednesday, August 23, 2017 Sheet 89 of 94

# BATTERY IN DETECT






<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_DETECT

Engineer: Adams Lin

| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 2.2 |

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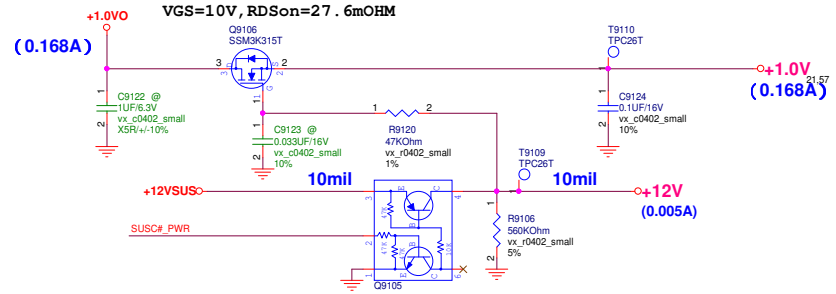
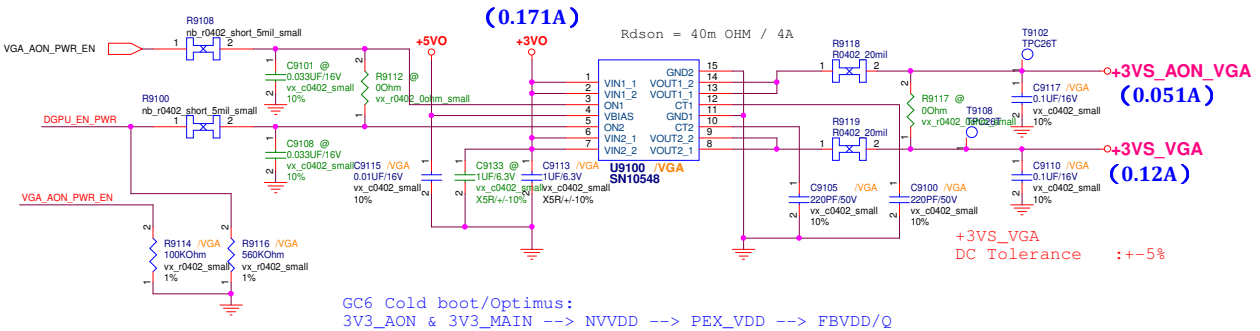
## SUSC#_PWR POWER

## SUSB#_PWR POWER

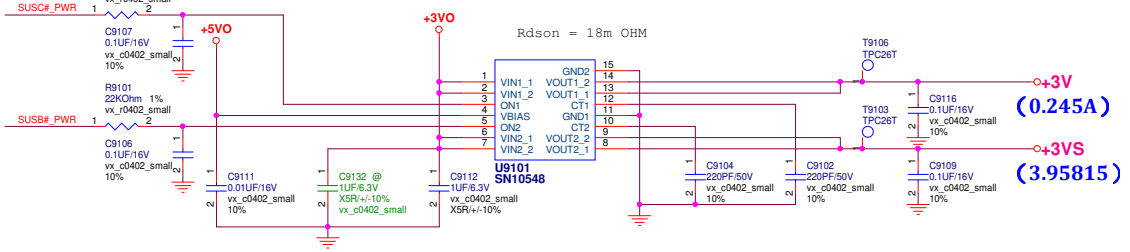



## DSC_VGA_PWR POWER




GC6 Cold boot/Optimus:
3V3_AON & 3V3_MAIN --> NVVDD --> PEX_VDD --> FBVDD/Q

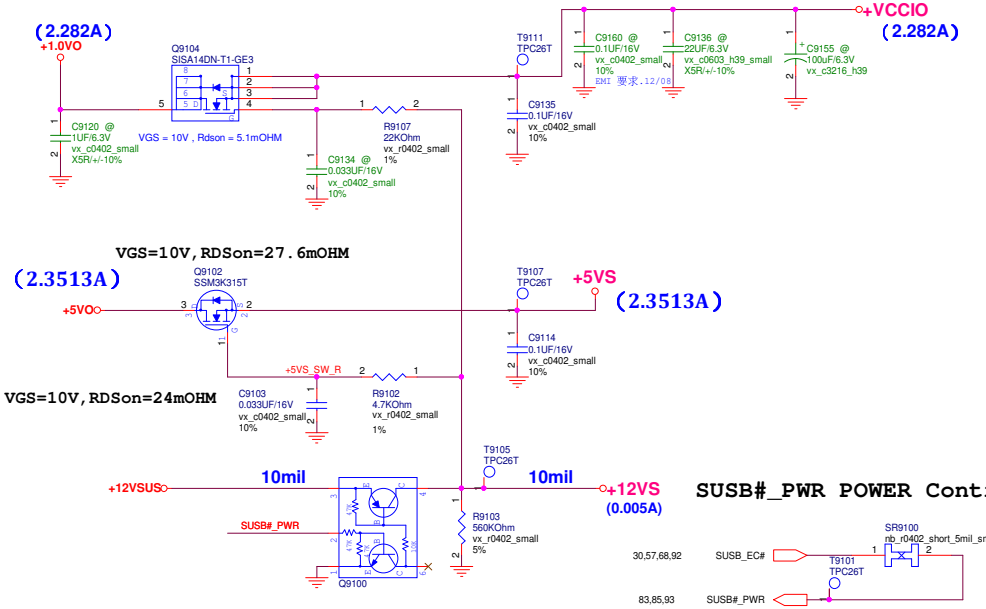
GC6 2.0 Exit:
3V3_MAIN --> NVVDD --> PEX_VDD




Power up Sequencing
1.The ramp time for any rail must be 40us and
is recommended to be less than 2ms
2.The previous power rail must ramp up to 90%
before the next power rail can start ramping up

Power down Sequencing
1.There is no specific power down sequence
2.Residual voltage from power down must not violate ther power up sequence
when back to back GPU power down and power up event take place

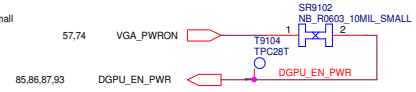




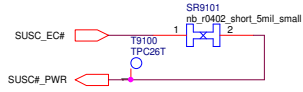

## DSC_VGA_PWR POWER Control

## SUSB#_PWR POWER Control




## SUSC#_PWR POWER Control




<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

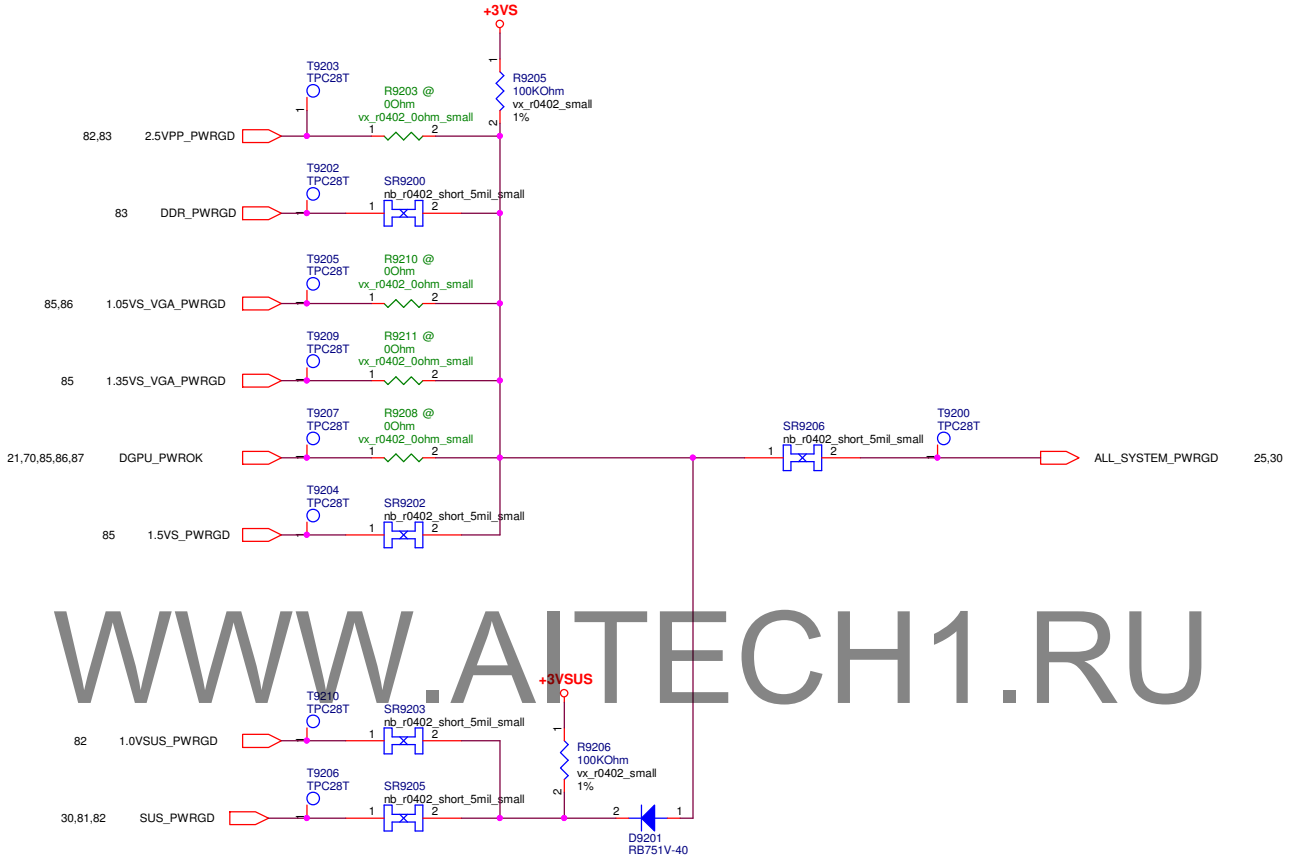
Title : POWER_LOAD SWITCH

Engineer: Adams Lin

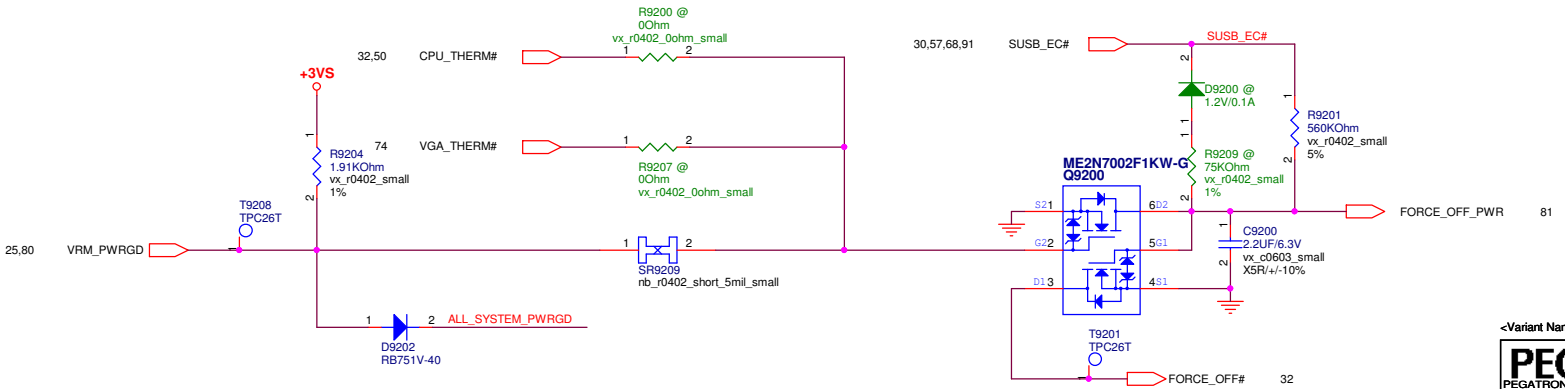
| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 2.2 |

Date: Wednesday, August 23, 2017 Sheet 91 of 94

# POWER GOOD DETECTER






<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_PROTECT

Engineer: Adams Lin

| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 2.2 |

Date: Wednesday, August 23, 2017 Sheet 92 of 94

+USB_PD_IN → +USB_PD_IN 42,89
+A/D_DOCK_IN → +A/D_DOCK_IN 60,89
+AC_USBPD_WCT_IN → +AC_USBPD_WCT_IN 88,89
+AC_BAT_SYS → +AC_BAT_SYS 41,43,45,80,81,82,83,85,87,88
+BAT_CON → +BAT_CON 60,88
+RTC_POWER → +RTC_POWER 81

+5VA → +5VA 31,56,81
+3VA → +3VA 24,30,31,36,43,53,56,57,67,81,88

+5VO → +5VO 26,81,82,83,85,88,91
+3VO → +3VO 81,82,84,85,86,91
+2.5VO → +2.5VO 82
+1.8VO → +1.8VO 84
+1.5VO → +1.5VO 85

+1.2VO → +1.2VO 83
+1.05VO_VGA → +1.05VO_VGA 86
+1.0VO → +1.0VO 82,91
+0.6VO → +0.6VO 83

+12VSUS → +12VSUS 81,91
+5VSUS → +5VSUS 41,42,52,56,67,81
+3VSUS → +3VSUS 4,24,25,26,28,30,31,33,42,51,53,62,67,68,81,92
+1.8VSUS → +1.8VSUS 9,21,24,26,84
+1.0VSUS → +1.0VSUS 26,82

+12V → +12V 91
+2P5VPP → +2P5VPP 16,17,57,82
+1.2V → +1.2V 4,7,15,16,17,18,57,83
+1.0V → +1.0V 7,57,91

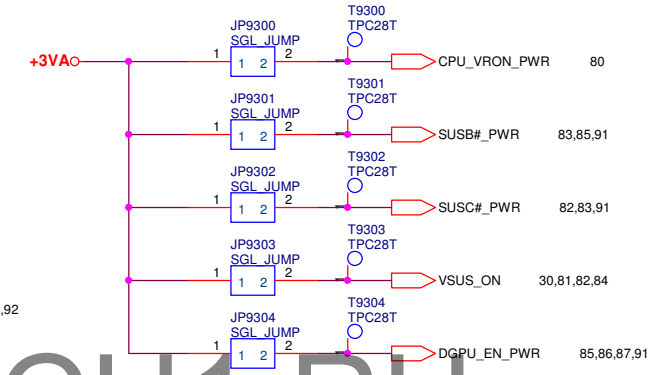
+12VS → +12VS 28,31,57,62,91
+5VS → +5VS 31,36,45,46,48,50,51,56,57,67,80,87,91
+3VS → +3VS 3,4,17,20,21,22,23,24,28,30,31,32,36,37,41,42,45,46,47,48,50,51,53,57,61,62,67,91,92

+1.5VS → +1.5VS 36,57,85

+1.05VS_VGA → +1.05VS_VGA 57,70,71,72,86
+0.6VS → +0.6VS 15,17,57,83

+VCORE → +VCORE 5,57,80
+VCCGT → +VCCGT 6,57,80
+VCCSA → +VCCSA 7,57,80
+VCCIO → +VCCIO 3,7,57,91
+VCCPRIM_CORE → +VCCPRIM_CORE 26,82
+VGA_VCORE → +VGA_VCORE 57,75,87

## FOR POWER TEST






PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

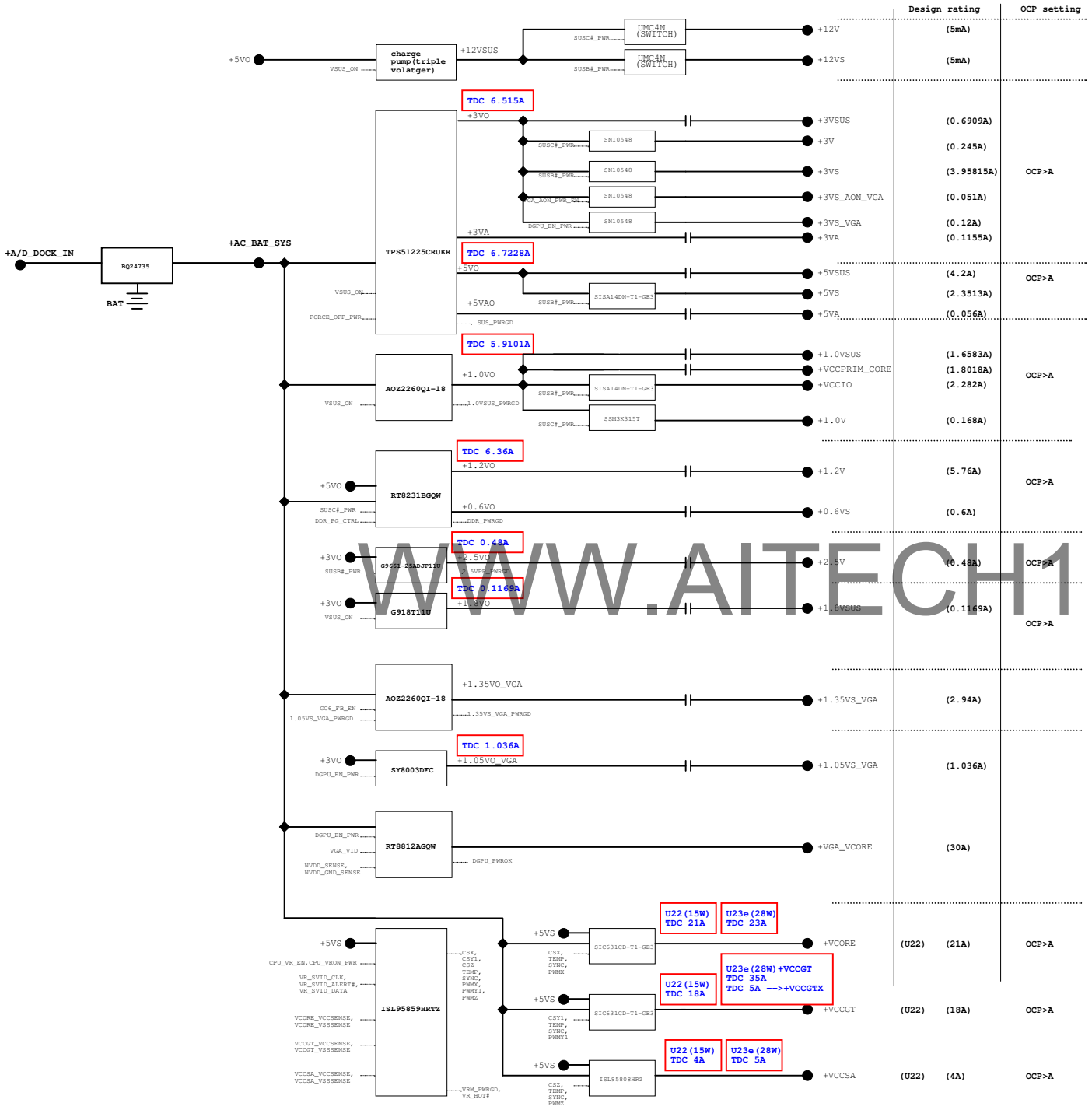
Title : POWER_SIGNAL

BG1-POWER

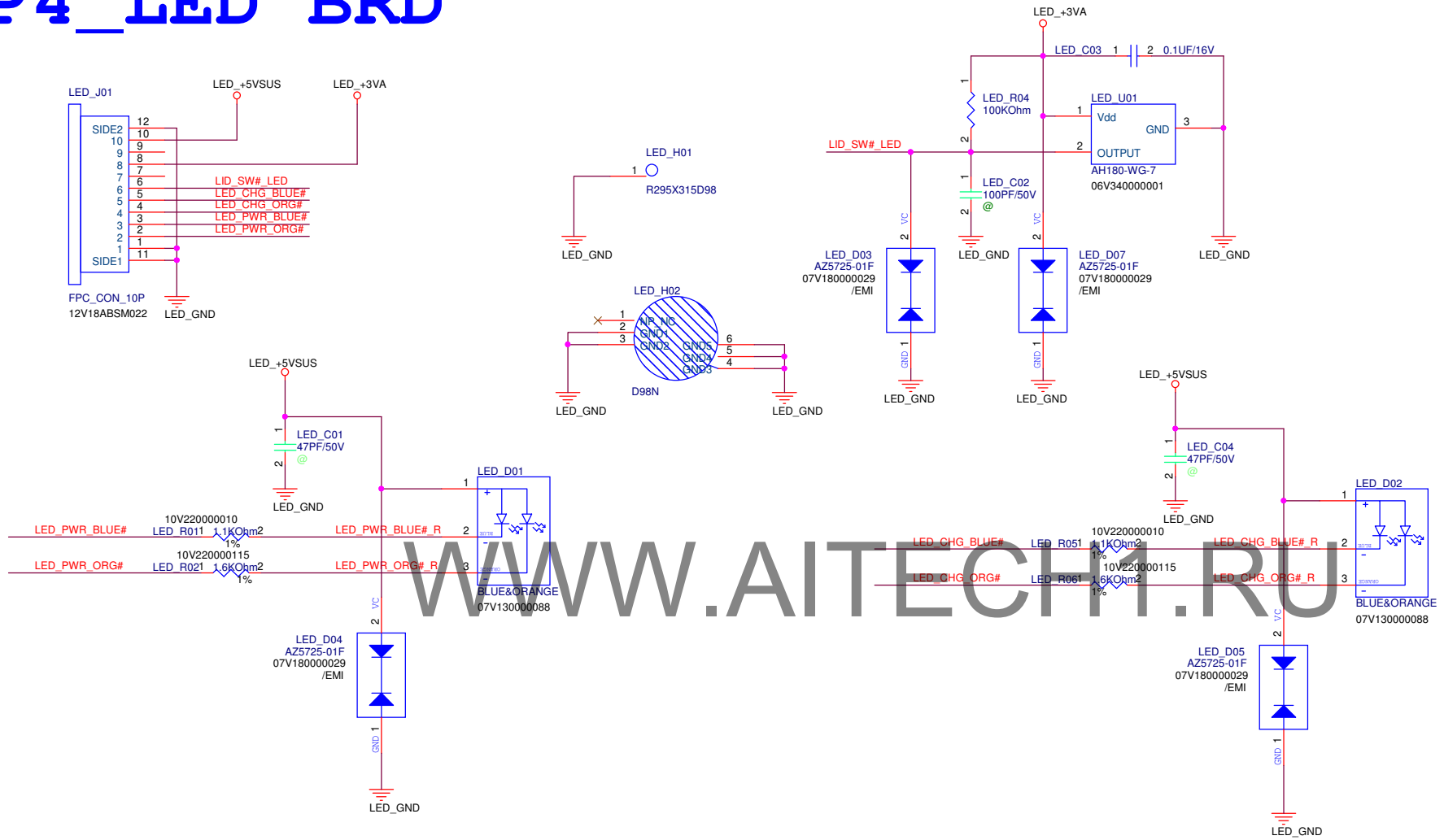
Engineer: Adams Lin

| Size | Project Name | Rev |
|---|---|---|
| B | AQ5EB | 2.2 |

Date: Wednesday, August 23, 2017 Sheet 93 of 94



# P4_LED BRD

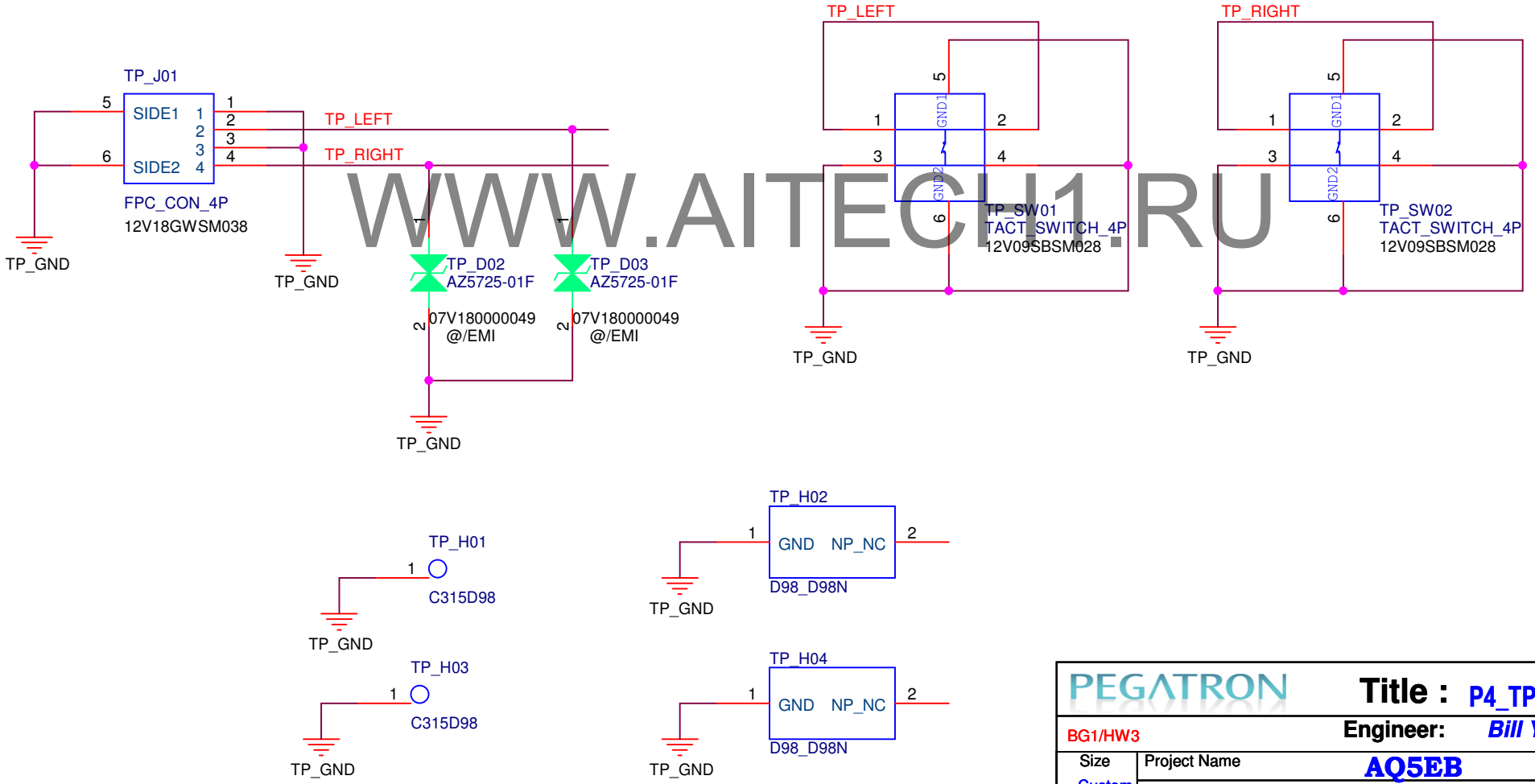





| | | |
|---|---|---|
| PEGATRON | Title : P4_LED BRD | |
| BG1/HW3 | Engineer: Bill Yang | |
| Size: Custom | Project Name: AQ5EB | Rev: 1.0 |
| | P/N | |
| Date: Wednesday, August 23, 2017 | Sheet 104 of 110 | |

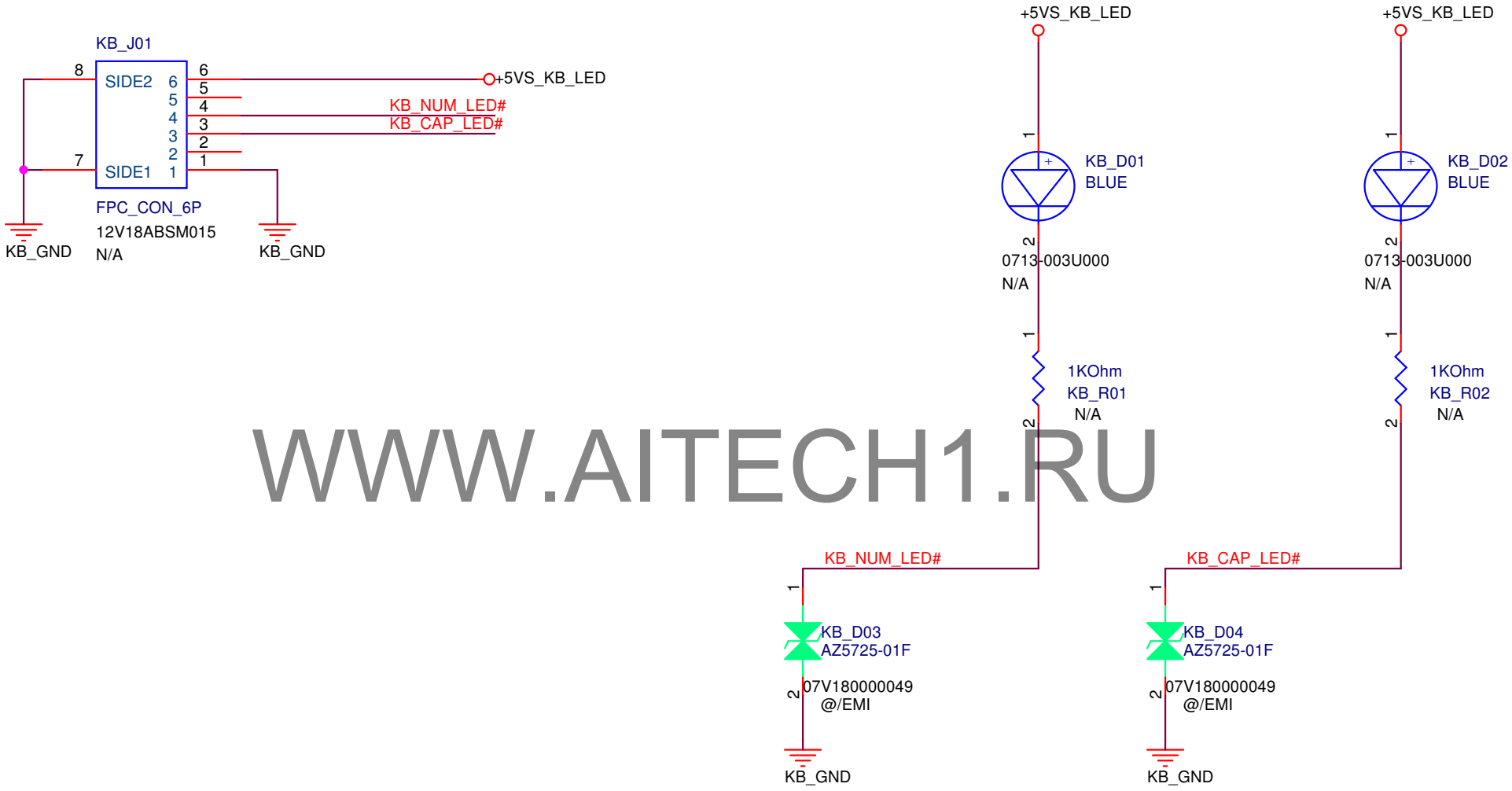
# P4_TP-button BRD

## TP_BRD to TP_Model

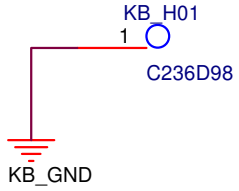





| | | |
|---|---|---|
| PEGATRON | Title : P4_TP-button BRD | |
| BG1/HW3 | Engineer: Bill Yang | |
| Size: Custom | Project Name: AQ5EB | Rev: 1.0 |
| | P/N: | |
| Date: Wednesday, August 23, 2017 | Sheet 105 of 110 | |






PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : P4_KB LED

Engineer: Bill Yang

BG1/HW3

| Size | Project Name | Rev |
|---|---|---|
| Custom | AQ5EB | 1.1 |

Date: Wednesday, August 23, 2017 Sheet 106 of 108